24

Semiconductor Electronics : Materials, Devices and Simple Circuits

Numerical

Q.1. From the given transfer characteristic of a transistor in CE configuration, the value of power gain of this configuration is 10^x, for RB=10 kΩ, and RC=1 kΩ. The value of x is _____.

JEE Main 2023 (Online) 13th April Morning Shift

Answer key & Explanation

1. Ans. Correct answer is 3

Explanation

Power gain

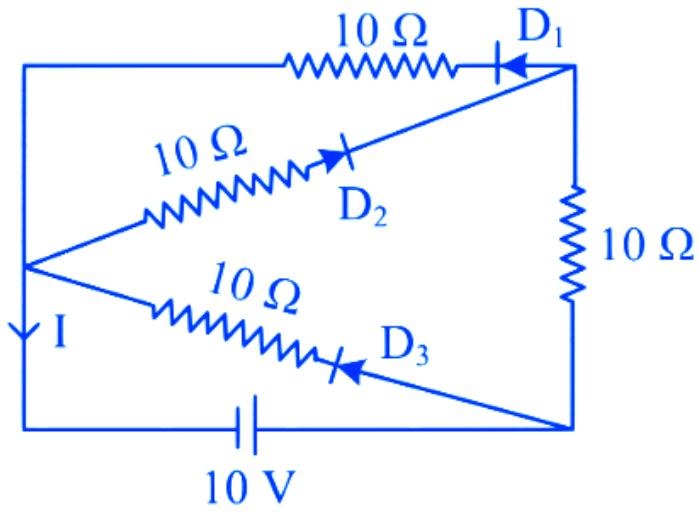
$$\Rightarrow A_v \cdot A_1 = B\frac{R_C}{R_B} \cdot B = B^2\frac{R_C}{R_B}$$

$$= \left(\frac{(20-10) \times 10^{-3}}{(200-100) \times 10^{-6}} \right) \times \frac{1 \times 10^{3}}{10 \times 10^{3}} = 10^{3}$$

Hence $\mathbf{x = 3}$

MCQ (Single Correct Answer)

Q.1. In the given circuit, the current (I) through the battery will be



A 1A

B 2.5 A

C 2 A

D 1.5 A

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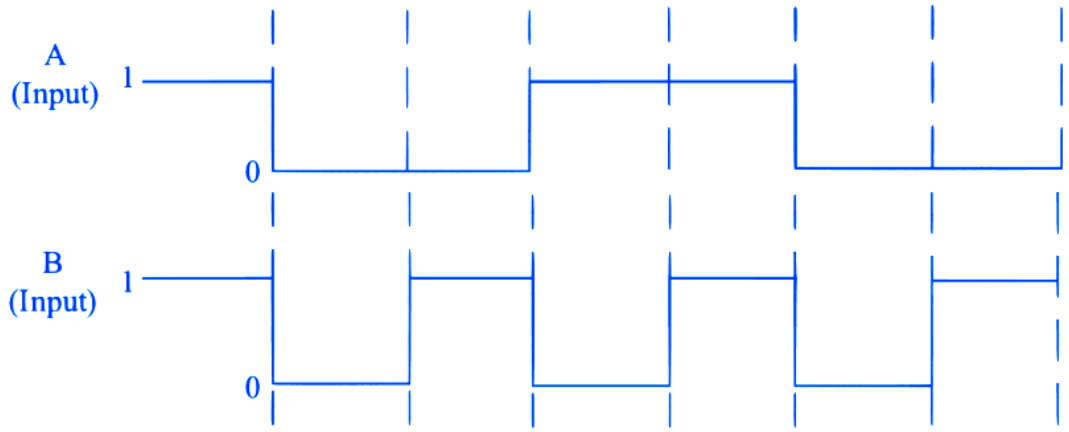
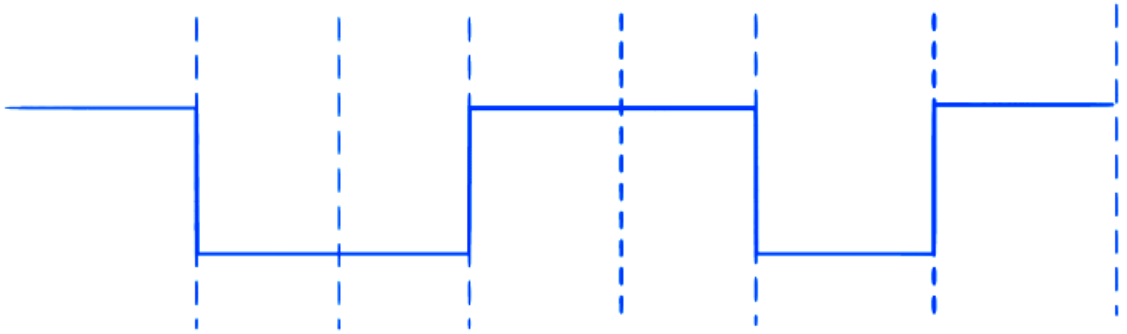
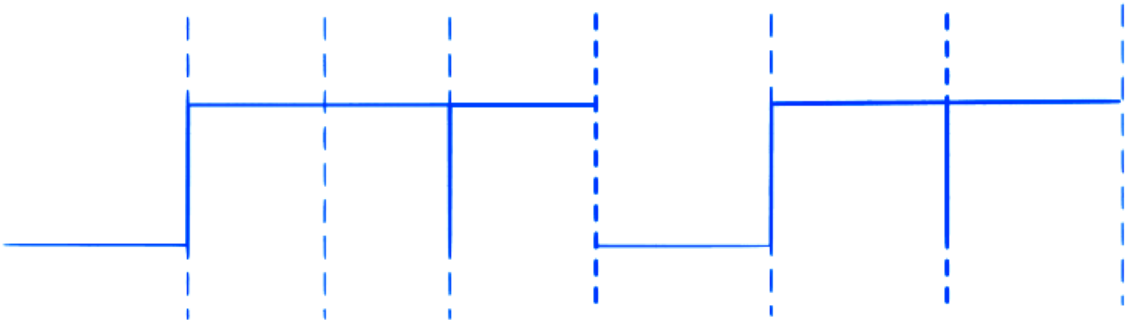
Q.2. The output from NAND gate having inputs A and B given below will be,



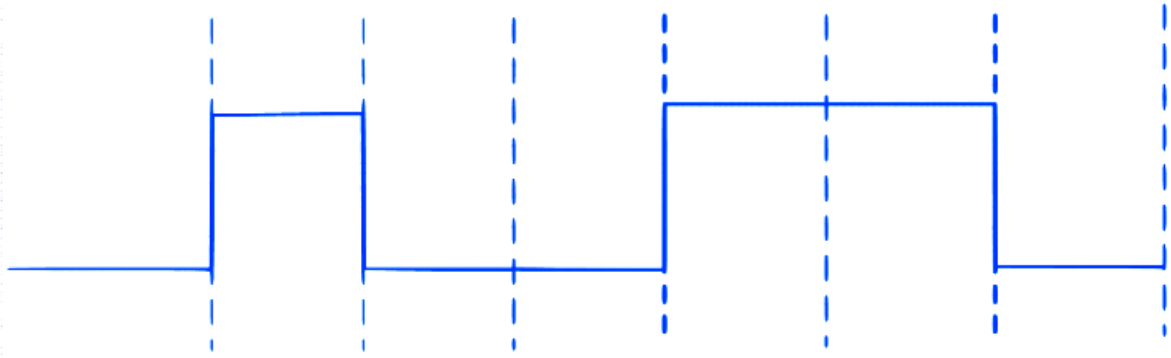
A



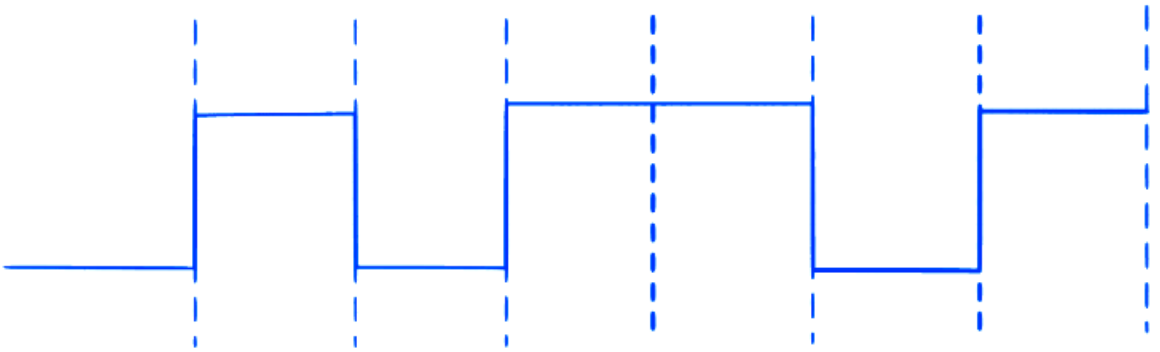
B



C



D



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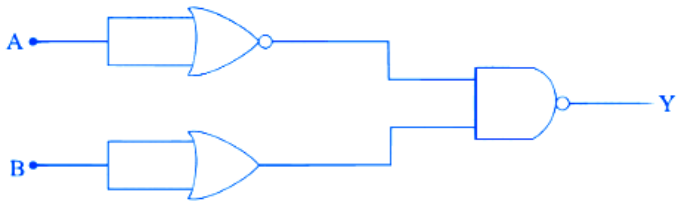
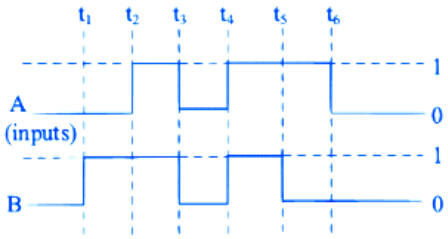
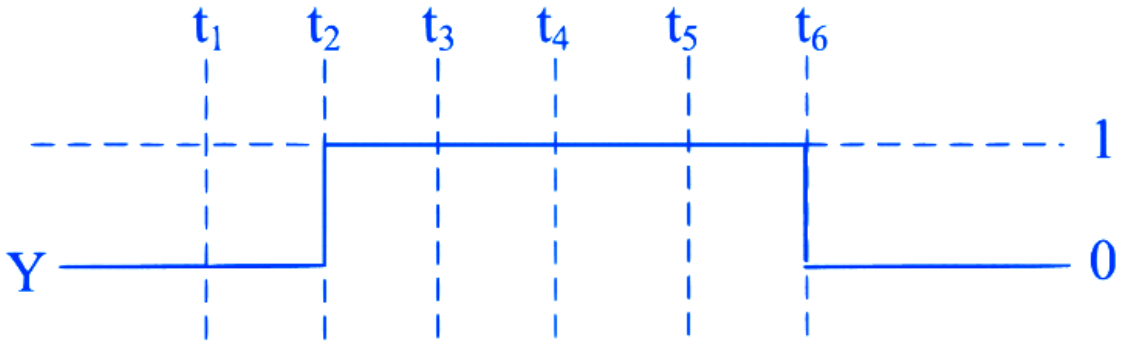
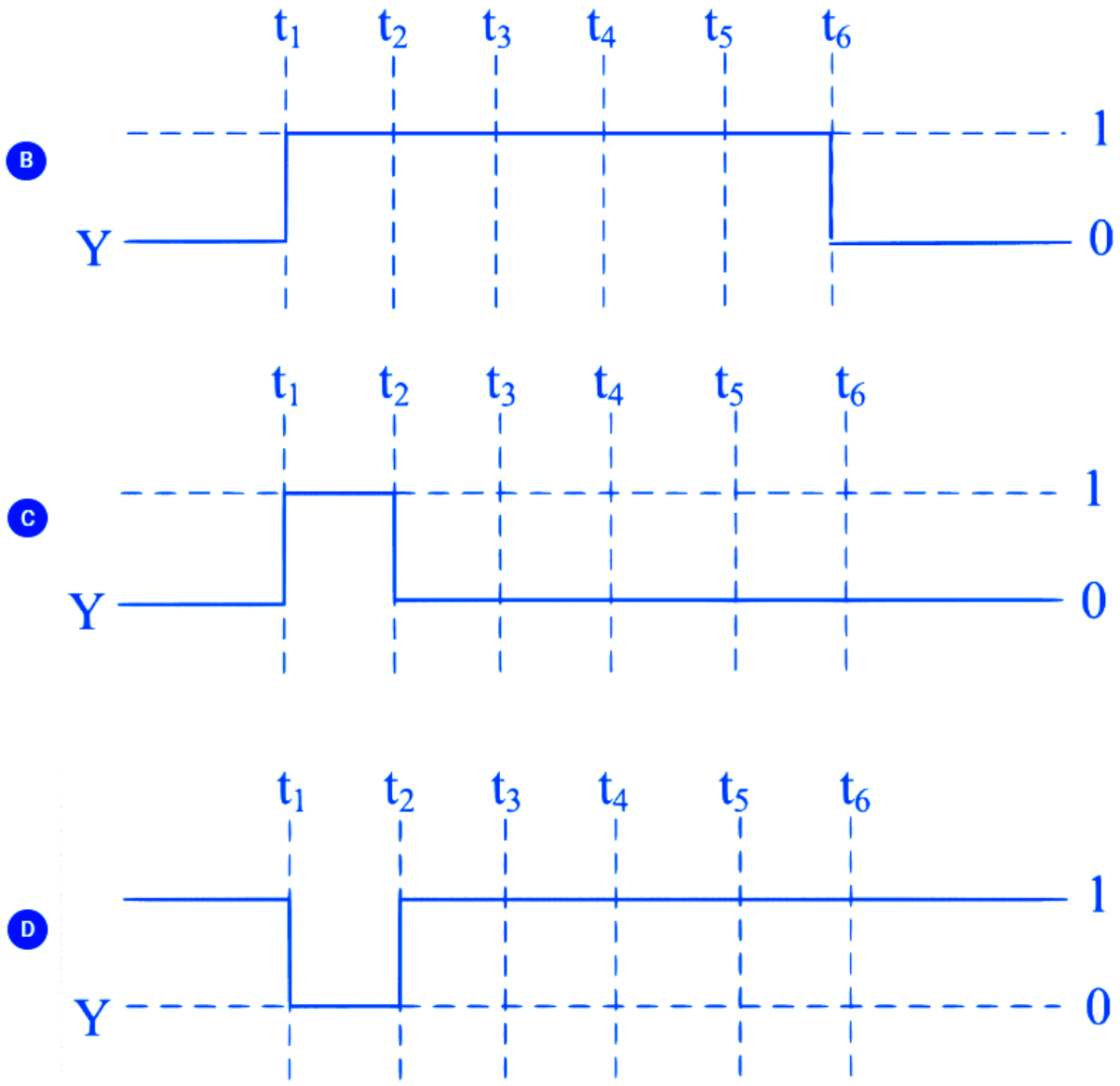
Q.3. For the following circuit and given inputs A and B, choose the correct option for output 'Y'





A





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Q.4. In an n-p-n common emitter (CE) transistor the collector current changes from 5 mA to 16 mA for the change in base current from 100 μA and 200 μA, respectively. The current gain of transistor is _____.

A 210

B 0.9

C 9

D 110

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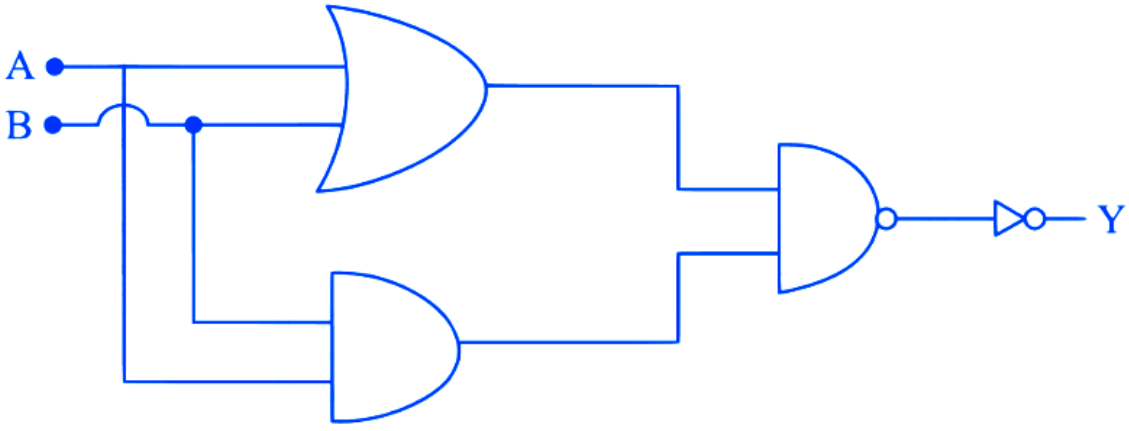
Q.5. The logic operations performed by the given digital circuit is equivalent to:



A NOR

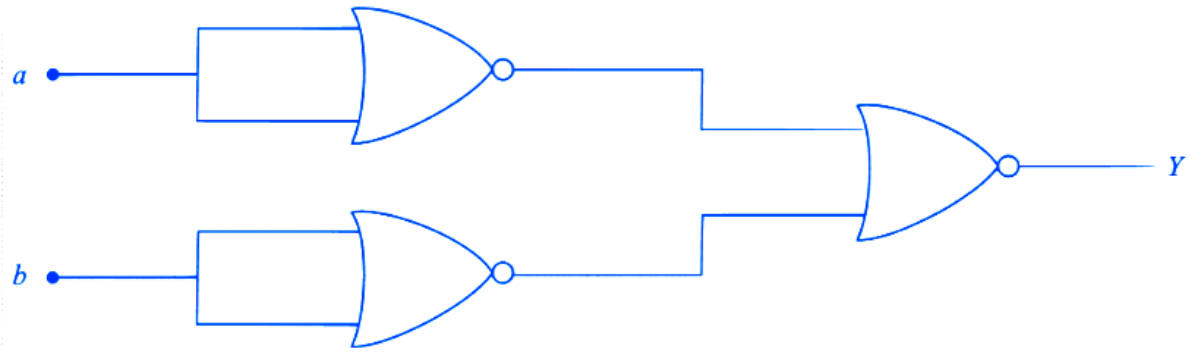
B AND

C NAND

D OR

JEE Main 2023 (Online) 11th April Evening Shift

Q.6. The logic performed by the circuit shown in figure is equivalent to :



A NAND

B AND

C OR

D NOR

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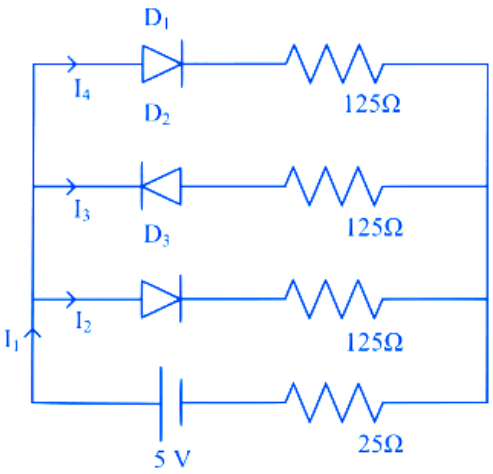
Q.7. If each diode has a forward bias resistance of 25 Ω in the below circuit,



Which of the following options is correct :

A $\frac{I_3}{I_4} = 1$

B $\frac{I_1}{I_2} = 2$

C $\frac{I_2}{I_3} = 1$

D $\frac{I_1}{I_2} = 1$

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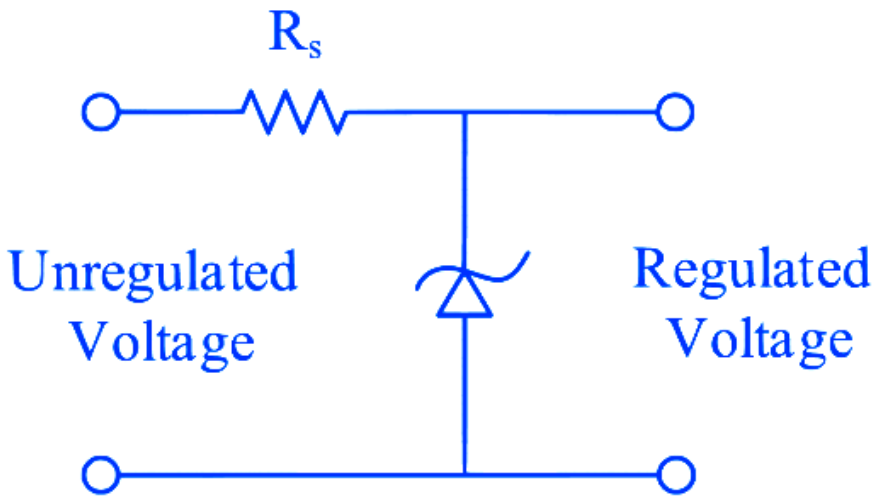
Q.8. A zener diode of power rating 1.6 W is to be used as voltage regulator. If the zener diode has a breakdown of 8V and it has to regulate voltage fluctuating between 3 V and 10 V. The value of resistance R_s for safe operation of diode will be



A $13\ \Omega$

B $13.3\ \Omega$

C $10\ \Omega$

D $12\ \Omega$

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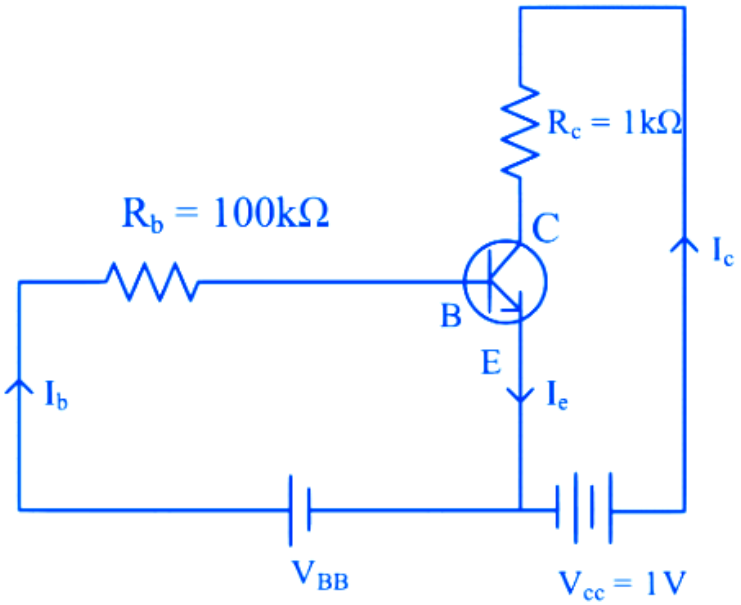
Q.9. For a given transistor amplifier circuit in CE configuration $V_{CC} = 1\,V, R_C = 1\,k\Omega, R_b = 100\,k\Omega$ and $\beta = 100$. Value of base current I_b is



A $I_b = 100\ \mu A$

B $I_b = 0.1\ \mu A$

C $I_b = 1.0\ \mu A$

D $I_b = 10\ \mu A$

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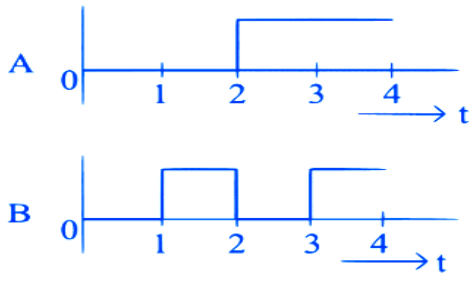
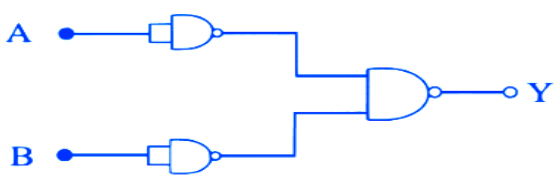
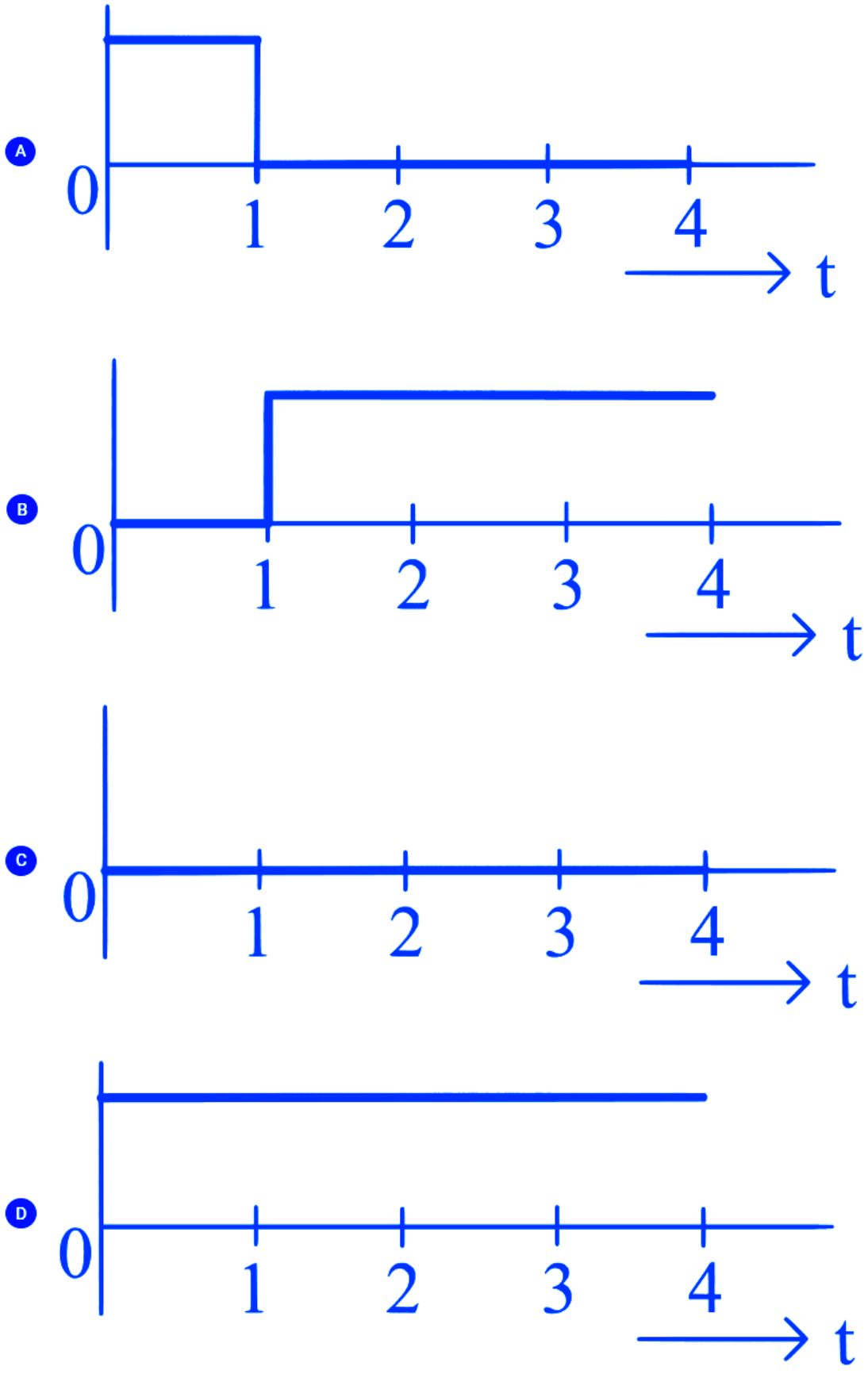
Q.10. For the logic circuit shown, the output waveform at Y is:







Q.11. Given below are two statements: one is labelled as Assertion A and the other is labelled as Reason R

Assertion A: Diffusion current in a p-n junction is greater than the drift current in magnitude if the junction is forward biased.

Reason R: Diffusion current in a p-n junction is from the n-side to the p-side if the junction is forward biased.

In the light of the above statements, choose the most appropriate answer from the options given below

(A) Both A and R are correct but R is NOT the correct explanation of A

(B) A is correct but R is not correct

(C) A is not correct but R is correct

(D) Both A and R are correct and R is the correct explanation of A

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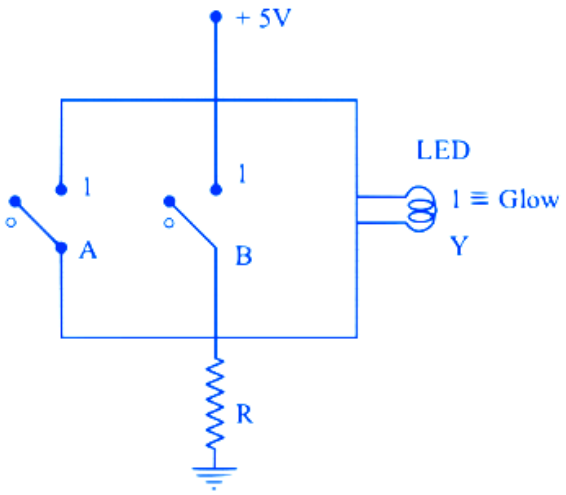
Q.12. Name the logic gate equivalent to the diagram attached



A NOR

B NAND

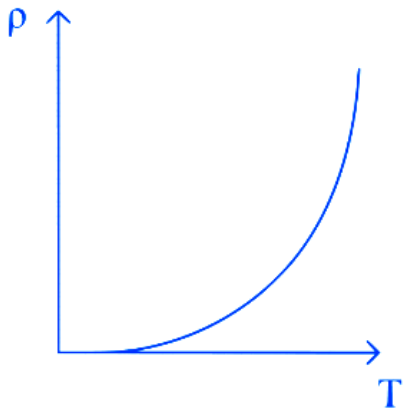
C AND

D OR

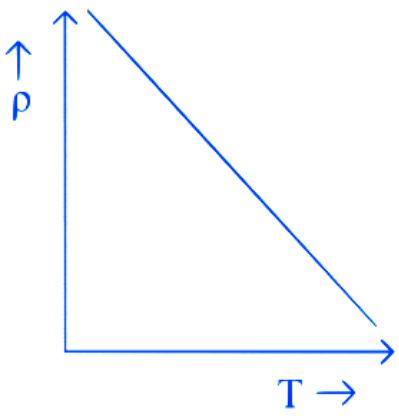
JEE Main 2023 (Online) 6th April Morning Shift

Q.13. The resistivity (p) of semiconductor varies with temperature. Which of the following curve represents the correct behaviour

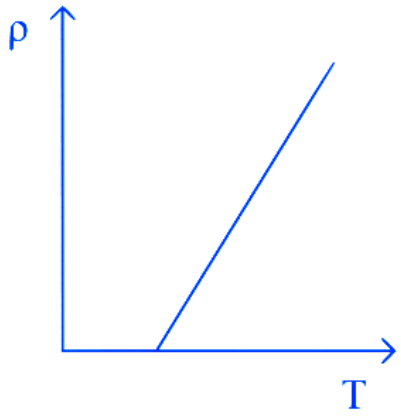
A



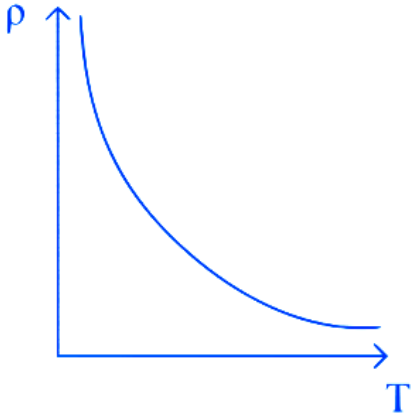
B



C



D



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Q.14. Choose the correct statement about Zener diode :

A It works as a voltage regulator in reverse bias and behaves like simple pn junction diode in forward bias.

B It works as a voltage regulator in both forward and reverse bias.

C It works as a voltage regulator only in forward bias.

D It works as a voltage regulator in forward bias and behaves like simple pn junction diode in reverse bias.

JEE Main 2023 (Online) 1st February Evening Shift

Q.15. Match List I with List II:

	List I		List II
A.	Intrinsic semiconductor	I.	Fermi-level near the valence bond
B.	n-type semiconductor	II.	Fermi-level in the middle of valence and conduction band.
C.	p-type semiconductor	III.	Fermi-level near the conduction band
D.	Metals	IV.	Fermi-level inside the conduction band

Choose the correct answer from the options given below :

A A-III, B-I, C-II, D-IV

B A-II, B-I, C-III, D-IV

C A-I, B-II, C-III, D-IV

D A-II, B-III, C-I, D-IV

JEE Main 2023 (Online) 1st February Morning Shift

Q.16. Given below are two statements :

Statement I: In a typical transistor, all three regions emitter, base and collector have same doping level.

Statement II: In a transistor, collector is the thickest and base is the thinnest segment.

In the light of the above statements, choose the most appropriate answer from the options given below.

A **Statement I** is correct but **Statement II** is incorrect

B Both **Statement I** and **Statement II** are incorrect

C **Statement I** is incorrect but **Statement II** is correct

D Both **Statement I** and **Statement II** are correct

JEE Main 2023 (Online) 31st January Evening Shift

Q.17. The effect of increase in temperature on the number of electrons in conduction band (ne) and resistance of a semiconductor will be as:

A n_e decreases, resistance increases

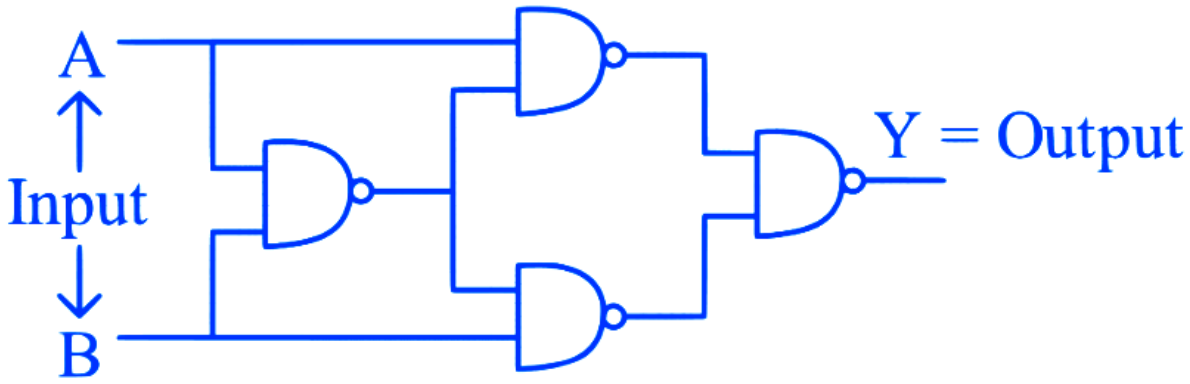
B Both n_e and resistance increase

C n_e increases, resistance decreases

D Both n_e and resistance decrease

JEE Main 2023 (Online) 31st January Morning Shift

Q.18. The output Y for the inputs A and B of circuit is given by



Truth table of the shown circuit is:

A

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

B

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

C

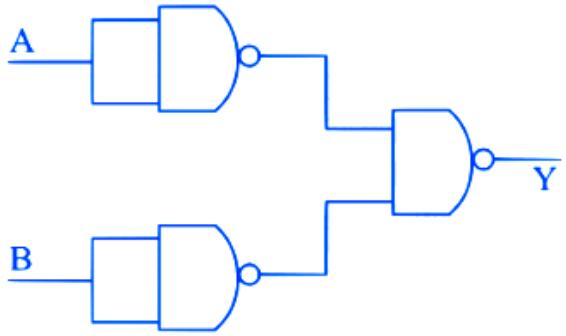
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

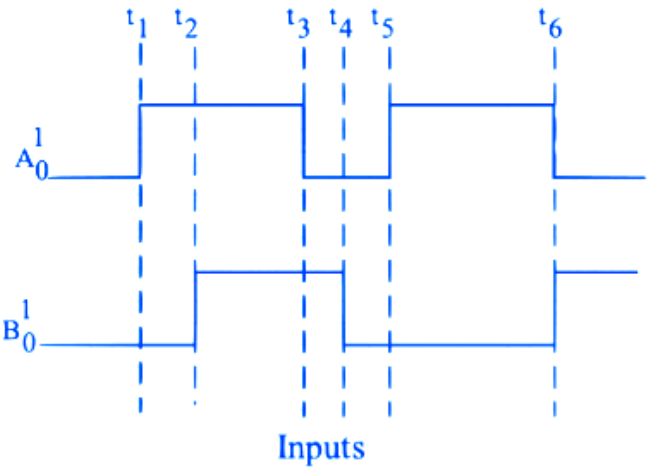
D

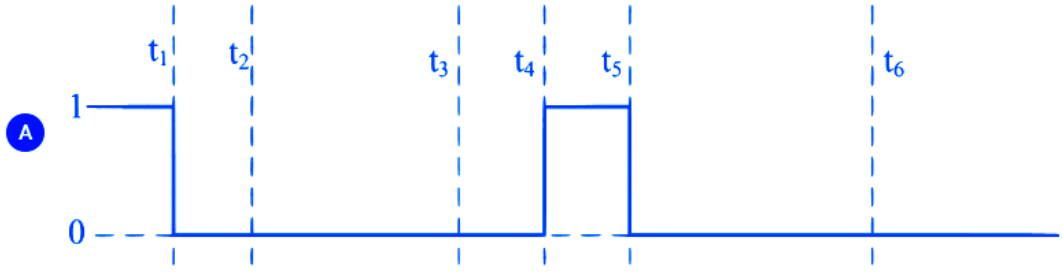
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

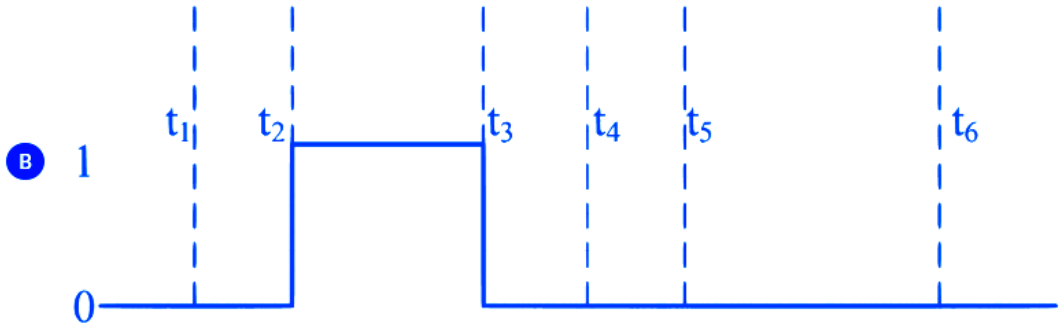
JEE Main 2023 (Online) 30th January Evening Shift

Q.19. The output waveform of the given logical circuit for the following inputs A and B as shown below, is :

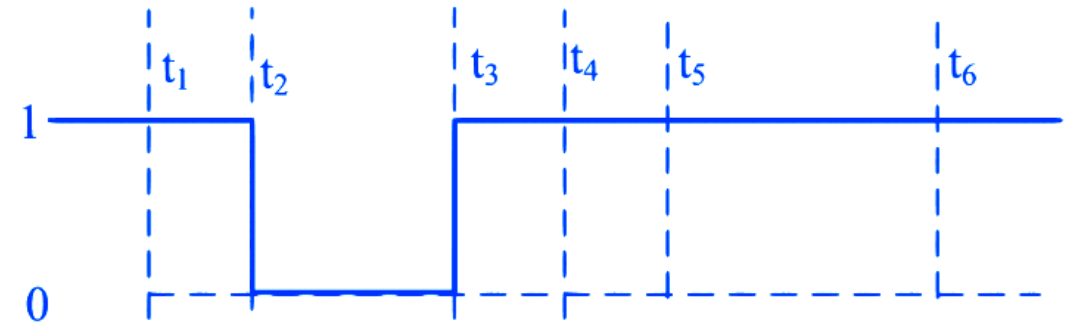




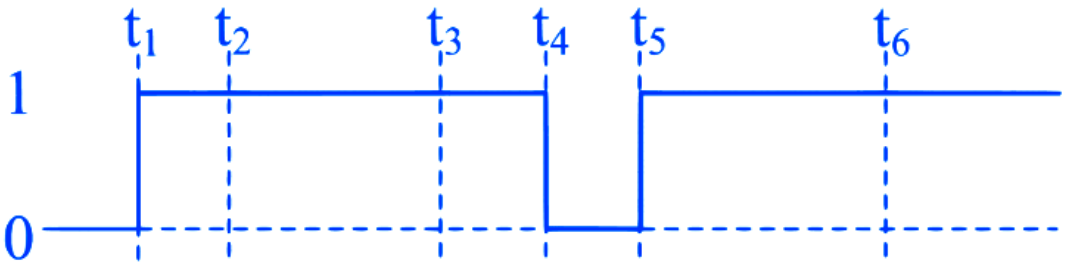




C

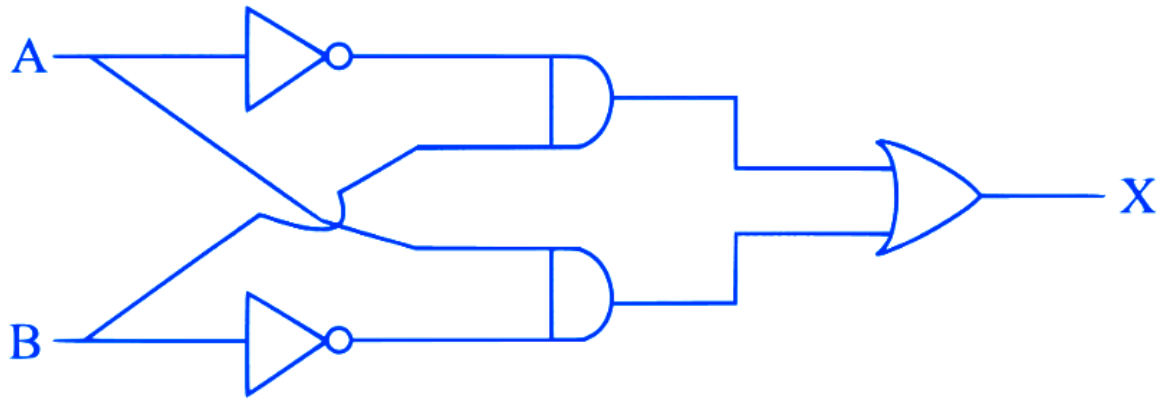


D



JEE Main 2023 (Online) 30th January Morning Shift

Q.20. For the given logic gates combination, the correct truth table will be



A

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

B

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

C

A	B	X
0	0	1
0	1	0
1	0	1
1	1	0

D

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

JEE Main 2023 (Online) 29th January Evening Shift

Q.21. Which one of the following Statement is **not** correct in the case of light emitting diodes?

A. It is a heavily doped p-n junction.

B. It emits light only when it is forward biased.

C. It emits light only when it is reverse biased.

D. The energy of the light emitted is equal to or slightly less than the energy gap of the semiconductor used.

Choose the correct answer from the options given below:

A A

B B

C C and D

D C

JEE Main 2023 (Online) 29th January Morning Shift

Q.22. Statement I : When a Si sample is doped with Boron, it becomes P type and when doped by Arsenic it becomes N-type semiconductor such that P-type has excess holes and N-type has excess electrons.

Statement II : When such P-type and N-type semi-conductors, are fused to make a junction, a current will automatically flow which can be detected with an externally connected ammeter.

In the light of above statements, choose the most appropriate answer from the options given below

A Statement I is incorrect but statement II is correct

B Both Statement I and statement II are correct

C Statement I is correct but statement II is incorrect

D Both Statement I and Statement II are incorrect

JEE Main 2023 (Online) 25th January Evening Shift

Q.23. Given below are two statements : one is labelled as Assertion A and the other is labelled as Reason R

Assertion A : Photodiodes are used in forward bias usually for measuring the light intensity.

Reason R : For a p-n junction diode, at applied voltage V the current in the forward bias is more than the current in the reverse bias for $|V_z| > \pm v \geq |v_0|$ where v_0 is the threshold voltage and V_z is the breakdown voltage.

In the light of the above statements, choose the correct answer from the options given below

A Both A and R are true but R is NOT the correct explanation of A

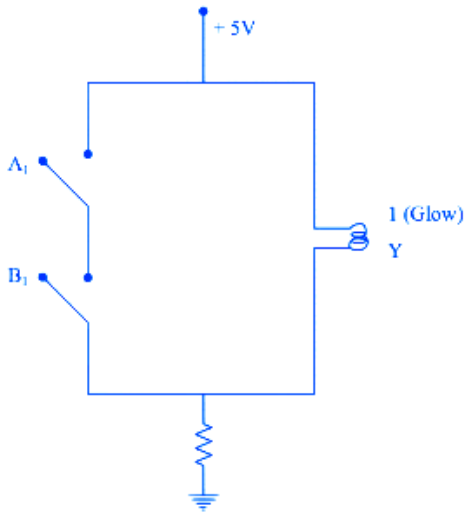
B A is true but R is false

C Both A and R are true and R is the correct explanation of A

D A is false but R is true

JEE Main 2023 (Online) 25th January Morning Shift

Q.24.



The logic gate equivalent to the given circuit diagram is :

A NOR

B OR

C NAND

D AND

JEE Main 2023 (Online) 24th January Evening Shift

Q.25. iven below are two statements : one is labelled as Assertion A and the other is labelled as Reason R

Assertion A : Photodiodes are preferably operated in reverse bias condition for light intensity measurement.

Reason R : The current in the forward bias is more than the current in the reverse bias for a p–n junction diode.

In the light of the above statements, choose the correct answer from the options given below

A Both A and R are true and R is the correct explanation of A

B A is false but R is true

C A is true but R is false

D Both A and R are true but R is NOT the correct explanation of A

JEE Main 2023 (Online) 24th January Morning Shift

Answer Key & Explanation

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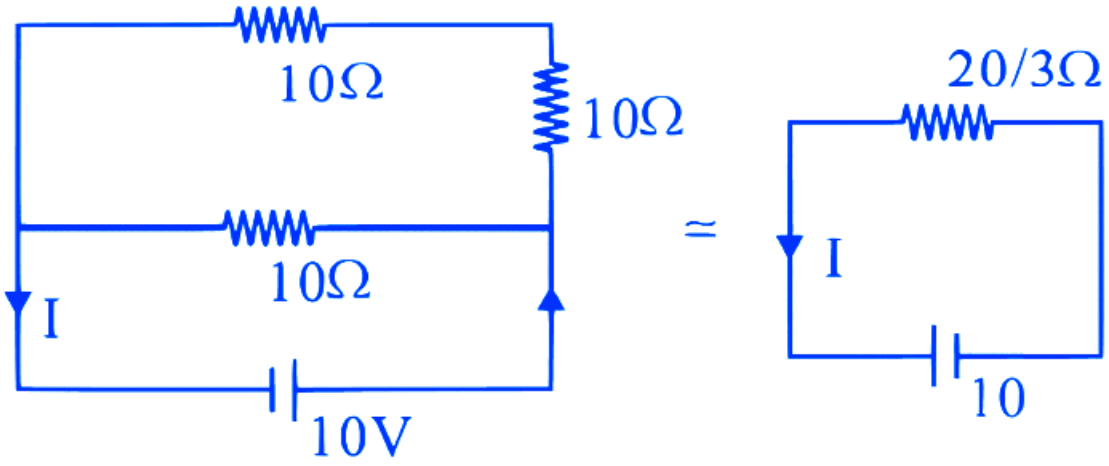
1. Ans. (D)

Explanation

In the circuit D1 and D3 are forward biased and D2 is reverse biased.



$$\therefore I = \frac{10}{20/3} = \frac{3}{2}\,A = 1.5\,A$$

2. Ans. (B)

Explanation

Truth table for NAND gate is

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

On the basis of given input A and B the truth table is

A	B	Y
1	1	0
0	0	1
0	1	1
1	0	1
1	1	0
0	0	1
0	1	1

3. Ans. (D)

Explanation

$$Y = (A' \cdot B)'$$

$$= A + B'$$

$$\Rightarrow \text{ Option } D.$$

4. Ans. (D)

Explanation

The current gain of a transistor in common emitter configuration is given by:

$$\beta = \frac{I_C}{I_B}$$

where I_C is the collector current and I_B is the base current.

In this case, the collector current changes from $5\,\text{mA}$ to $16\,\text{mA}$ for the change in base current from $100\,\mu\text{A}$ to $200\,\mu\text{A}$. Therefore, we have:

$$\Delta I_C = 16\,\text{mA} - 5\,\text{mA} = 11\,\text{mA}$$

$$\Delta I_B = 200\,\mu\text{A} - 100\,\mu\text{A} = 100\,\mu\text{A}$$

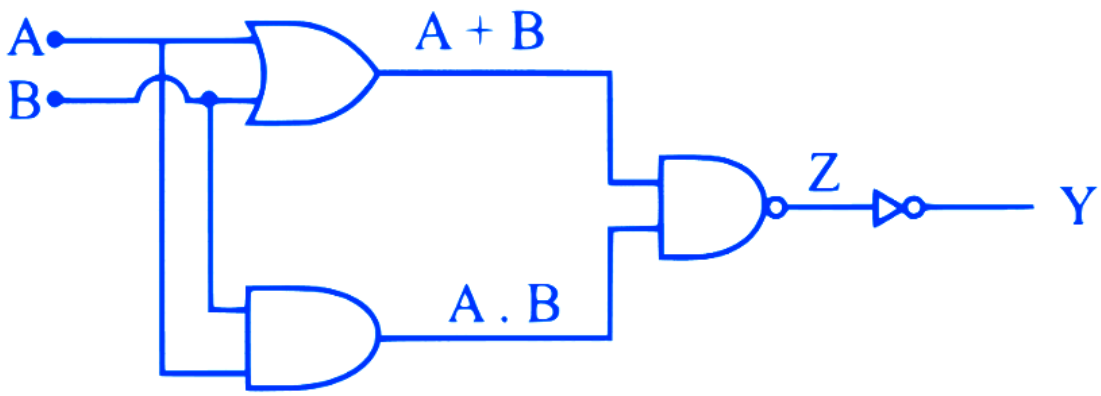
Therefore, the current gain of the transistor is:

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{11\,\text{mA}}{100\,\mu\text{A}} = 110$$

Therefore, the current gain of the transistor is 110.

5. Ans. (B)

Explanation



$$Z = \overline{(A + B) \cdot (A \cdot B)}$$

$$Y = \bar{Z} = (A + B) \cdot (A \cdot B)$$

$$Y = A \cdot (AB) + B \cdot (AB)$$

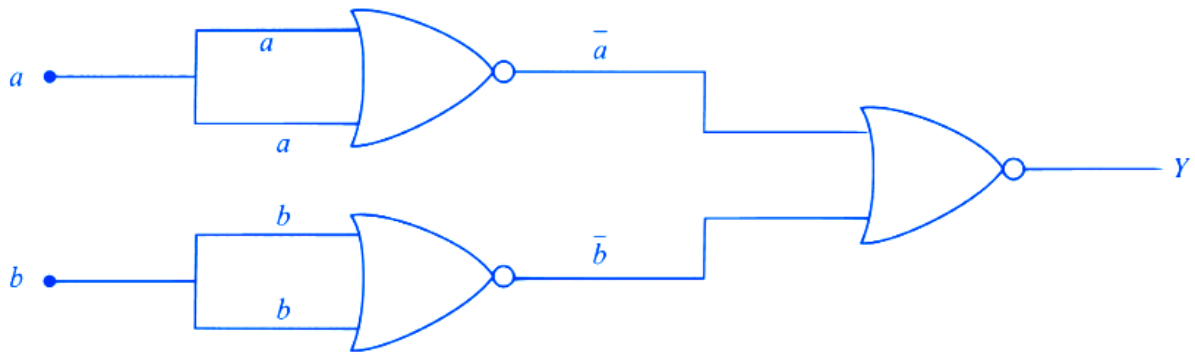
$$= AB + AB$$

$$= (AB)$$

$\therefore$ It is an AND gate.

6. Ans. (B)

Explanation



$$Y = \overline{\bar{a} + \bar{b}} = a \cdot b$$

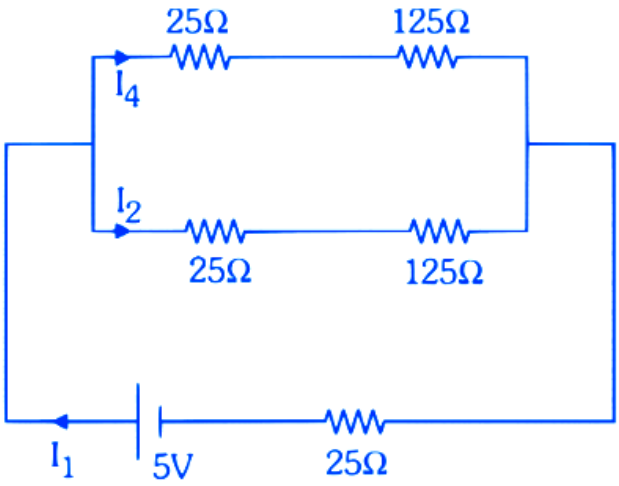
The truth table for the given circuit will be

a	b	output
0	0	0
0	1	0
1	0	0
1	1	1

Hence it will be equivalent to **AND** gate.

7. Ans. (B)

Explanation



$$R_{eq} = \frac{150 \times 150}{300} + 25 = 100\Omega$$

$$I_1 = \frac{5}{10} = 0.05\ A$$

$$I_2 = I_4 = \frac{0.05}{2} = 0.025\ A$$

$$\frac{I_1}{I_2} = 2$$

8. Ans. (C)

9. Ans. (D)

10. Ans. (B)

11. Ans. (B)

Explanation

A p-n junction consists of a p-type semiconductor (which has an excess of holes) in contact with an n-type semiconductor (which has an excess of electrons). In a forward-biased p-n junction, an external voltage is applied such that the positive terminal is connected to the p-side and the negative terminal is connected to the n-side. This configuration promotes the flow of majority charge carriers (holes from the p-side and electrons from the n-side) across the junction.

There are two types of currents in a p-n junction: drift current and diffusion current. Drift current is caused by the electric field due to the built-in potential, which opposes the flow of majority charge carriers. Diffusion current is caused by the concentration gradient of the charge carriers, which promotes the flow of majority charge carriers.

When the p-n junction is forward biased, the applied voltage reduces the potential barrier, allowing more majority charge carriers to flow across the junction. This results in an increase in the diffusion current. In a forward-biased p-n junction, the diffusion current is indeed greater than the drift current in magnitude, so **Assertion A** is correct.

Regarding **Reason R**: The diffusion current in a p-n junction is actually from the p-side to the n-side, as holes (majority charge carriers in the p-side) move from the p-side to the n-side, and

electrons (majority charge carriers in the n-side) move from the n-side to the p-side. Therefore, Reason R is incorrect.

12. Ans. (A)

13. Ans. (D)

14. Ans. (A)

Explanation

Option A is the correct statement about Zener diode. It works as a voltage regulator in reverse bias and behaves like a simple pn junction diode in forward bias. When a Zener diode is reverse-biased, it operates in the breakdown region, where a relatively constant voltage is maintained across the diode, regardless of the current flowing through it. This property makes it useful as a voltage regulator. In forward bias, the voltage applied across the diode is in the same direction as the normal direction of current flow. In this condition, the Zener diode behaves like a simple pn junction diode and allows current to flow in the forward direction.

15. Ans. (D)

Explanation

(A) Intrinsic semiconductor → II

(B) n-type semiconductor → III

(C) p-type semiconductor →1

(D) Metals → IV

16. Ans. (C)

Explanation

Emitter	Base	Collector
Moderate size	Thin	Thick
Maximum Doping	Minimum Doping	Moderate Doping

17. Ans. (C)

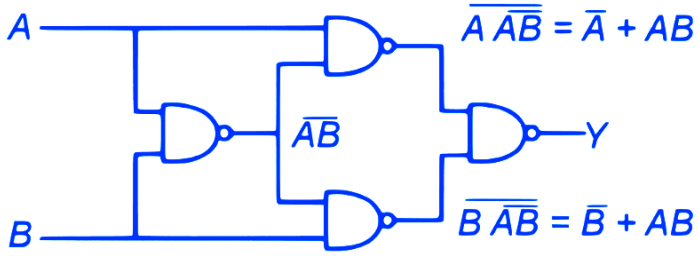
Explanation

As temperature increases n_e increases, this results in increase in conductance.

$\therefore T$ increases, n_e increases and R decreases.

18. Ans. (A)

Explanation



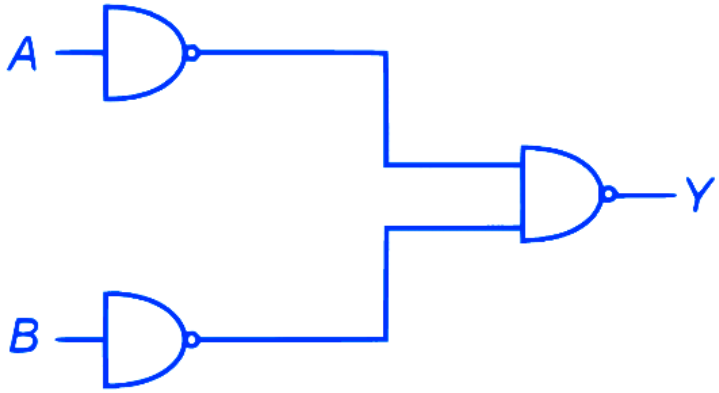
$$Y = \overline{\left(\overline{A} + AB\right)\left(\overline{B} + AB\right)} = (A + B)\left(\overline{A} + \overline{B}\right)$$

$= A\overline{B} + B\overline{A}$ (XOR gate)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

19. Ans. (D)

Explanation



Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

OR Gate

20. Ans. (D)

Explanation

As per the circuit,

$$X = A'B + AB'$$

If : $A = 0, B = 0 \Rightarrow X = 0$

$A = 0, B = 1 \Rightarrow X = 1$

$A = 1, B = 0 \Rightarrow X = 1$

$A = 1, B = 1 \Rightarrow X = 0$

21. Ans. (D)

Explanation

The correct answer is C. It is not correct that a light-emitting diode (LED) emits light only when it is reverse biased. In fact, an LED emits light only when it is forward biased, which is stated correctly in option B.

Option A is also correct, as an LED is indeed a heavily doped p-n junction. Option D is also correct, as the energy of the light emitted by an LED is equal to or slightly less than the energy gap of the semiconductor material used in the device.

Therefore, the statement that is not correct in the case of light-emitting diodes is C.

22. Ans. (C)

Explanation

Statement I is correct but in statement II we cannot detect the current through ammeter thus the statement II is incorrect.

23. Ans. (D)

Explanation

Photodiodes are used in reverse bias therefore the assertion is incorrect.

24. Ans. (C)

Explanation

The truth table for the circuit will be given as below

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

The above truth table is of NAND Gate.

25. Ans. (D)

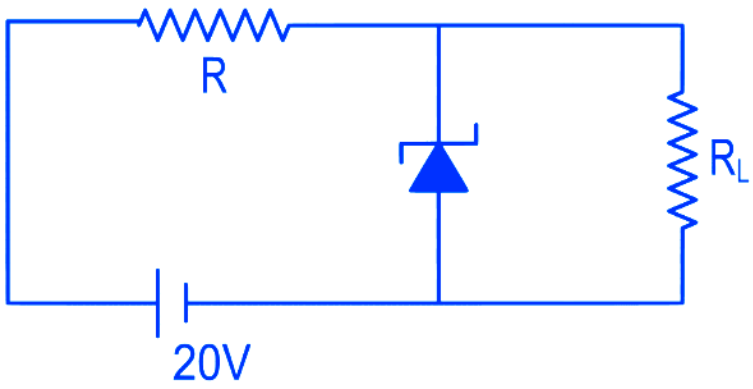
Explanation

Photodiodes are preferably operated in reverse bias condition for light intensity measurement because it increases the width of depletion layer, therefore both are correct but not the correct explanation.

2022

Numerical

Q.1. A 8 V Zener diode along with a series resistance R is connected across a 20 V supply (as shown in the figure). If the maximum Zener current is 25 mA, then the minimum value of R will be _____ Ω.



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Q.2. If the potential barrier across a p-n junction is 0.6 V. Then the electric field intensity, in the depletion region having the width of 6×10–6 m, will be _____ ×105 N/C.

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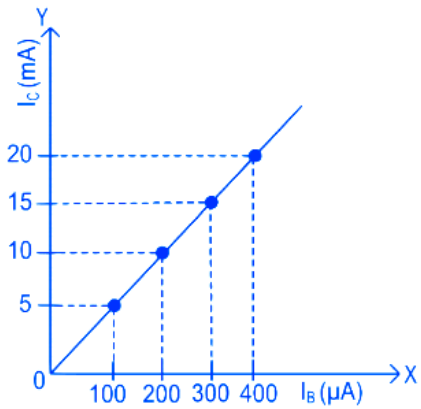
Q.3. The typical transfer characteristics of a transistor in CE configuration is shown in figure. A load resistor of 2$k\Omega$ is connected in the collector branch of the circuit used. The input resistance of the transistor is 0.50kΩ. The voltage gain of the transistor is _____.



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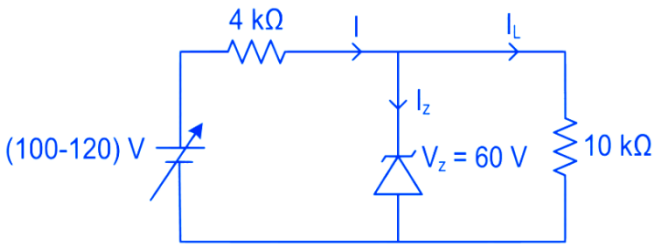
Q.4. In the circuit shown below, maximum zener diode current will be _____ mA.



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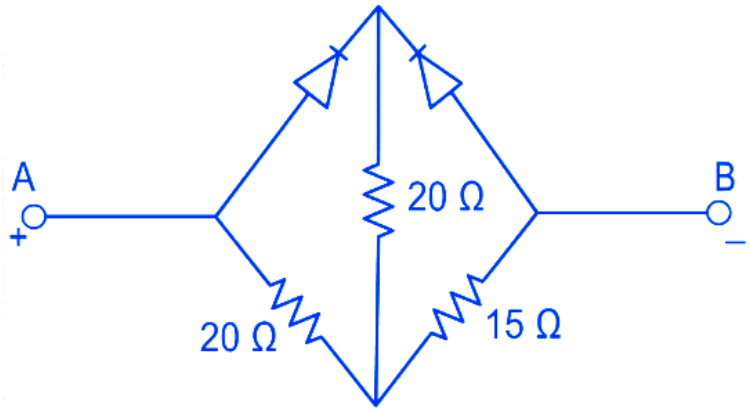
Q.5. Two ideal diodes are connected in the network as shown in figure. The equivalent resistance between A and B is _____ Ω.



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Q.6. The energy band gap of semiconducting material to produce violet (wavelength = 4000Aº) LED is _____ eV. (Round off to the nearest integer).

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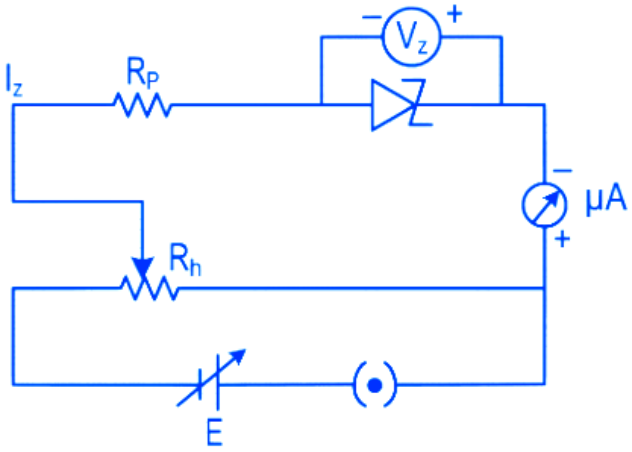
Q.7. The circuit diagram used to study the characteristic curve of a zener diode is connected to variable power supply (0 – 15 V) as shown in figure. A zener diode with maximum potential V_z = 10 V and maximum power dissipation of 0.4 W is connected across a potential divider arrangement. The value of resistance R_P connected in series with the zener diode to protect it from the damage is _____ Ω.



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Q.8. A potential barrier of 0.4 V exists across a p-n junction. An electron enters the junction from the n-side with a speed of 6.0×10^5 ms^{-1}. The speed with which electron enters the p side will be $x/3 \times 105$ ms^{-1} the value of x is _____.

(Given mass of electron = 9×10^{-31} kg, charge on electron = 1.6×10^{-19} C.)

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Q.9. A transistor is used in an amplifier circuit in common emitter mode. If the base current changes by 100 μA, it brings a change of 10 mA in collector current. If the load resistance is 2 kΩ and input resistance is 1 kΩ, the value of power gain is $x \times 10^4$. The value of x is _____.

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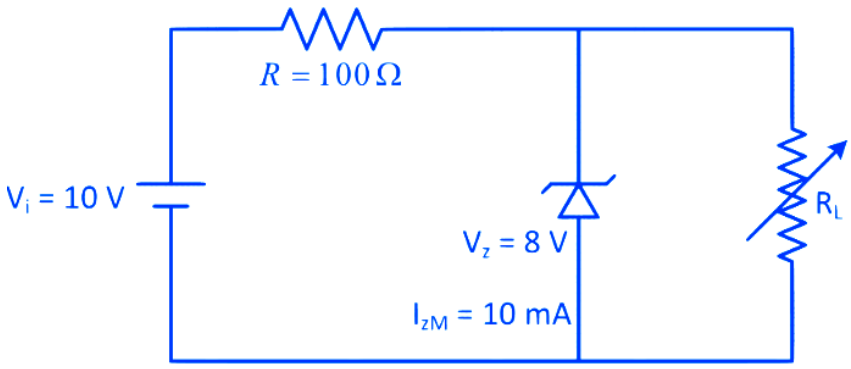
Q.10. A zener of breakdown voltage V_z = 8 V and maximum zener current, I_{ZM} = 10 mA is subject d to an input voltage V_i = 10 V with series resistance R = 100 Ω. In the given circuit R_L represents the variable load resistance. The ratio of maximum and minimum value of R_L is _____.



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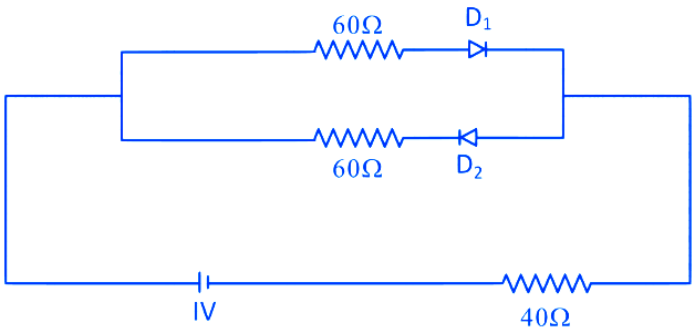
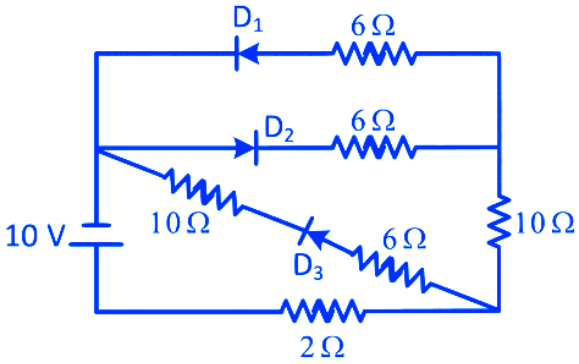
Q.11. The cut-off voltage of the diodes (shown in figure) in forward bias is 0.6 V. The current through the resister of 40 Ω is _____ mA.



JEE Main 2022 (Online) 27th June Evening Shift

Q.12. As per the given circuit, the value of current through the battery will be _____ A.



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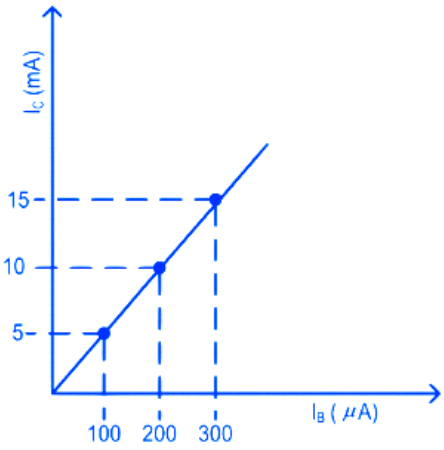
Q.13. In an experiment of CE configuration of n-p-n transistor, the transfer characteristics are observed as given in figure.



If the input resistance is 200 Ω and output resistance is 60 Ω, the voltage gain in this experiment will be _____.

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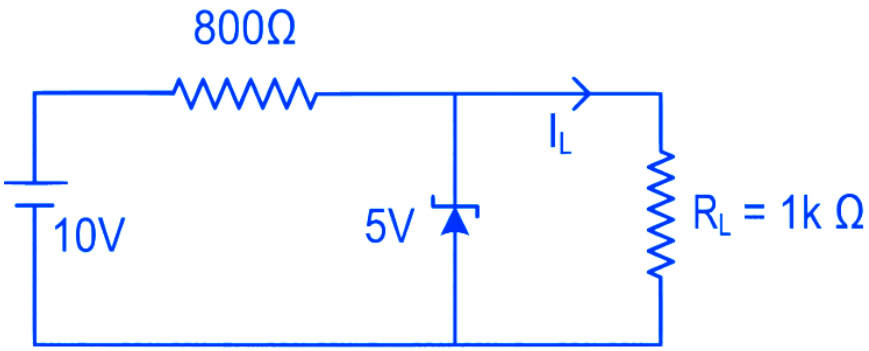
Q.14. In the given circuit, the value of current I_L will be _____ mA. (When R_L = 1kΩ)



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Q.15. A transistor is used in common-emitter mode in an amplifier circuit. When a signal of 10 mV is added to the base-emitter voltage, the base current changes by 10 μA and the collector current changes by 1.5 mA. The load resistance is 5 kΩ. The voltage gain of the transistor will be _____.

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Answer Key & Explanation

1. Ans. Correct answer is 480

Explanation

R will be minimum when R_L is infinitely large, so

$$R_{\text{Zener}} = \frac{8}{25\times10^{-3}} = 320\Omega$$

So $\frac{R}{R_{\text{Zener}}} = \frac{12}{8}$

$$R = \frac{12}{8} \times 320 = 480\Omega$$

2. Ans. Correct answer is 1

Explanation

$$E = \frac{V}{d} = \frac{0.6}{6\times10^{-6}} = 1 \times 10^5$$

3. Ans. Correct answer is 200

Explanation

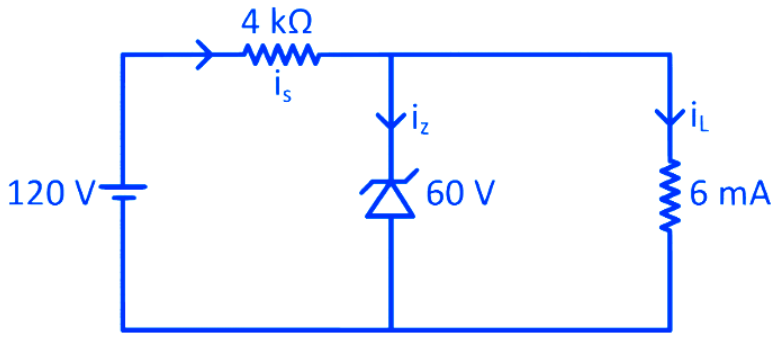
V_{gain} = Current gain $\times \frac{R_L}{R_i}$

$$= \frac{\Delta I_C}{\Delta I_B} \times \frac{R_L}{R_i}$$

$$= \frac{5\times10^{-3}}{100\times10^{-6}} \times \frac{2\times10^3}{0.5\times10^3} = \frac{10}{0.5} \times 10 = 200$$

4. Ans. Correct answer is 9

Explanation



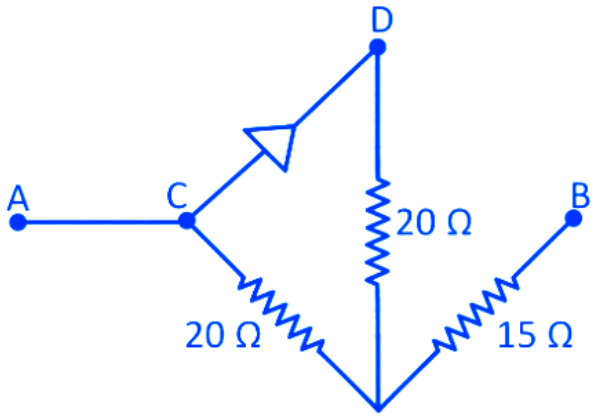
$$i_s = \frac{60}{4\times10^3} = 15\times10^{-3} = 15\,\text{mA}$$

$$i_L = \frac{60}{10\times10^3} = 6\,\text{mA}$$

$$I_z = i_s - i_L = 9\,\text{mA}$$

5. Ans. Correct answer is 25

Explanation



$$R = \frac{20\times20}{40} + 15 = 25\,\Omega$$

6. Ans. Correct answer is 3

Explanation

Energy corresponding to wavelength 4000 $\overset{o}{A}$

$$E = \frac{hc}{\pi}$$

$$= \frac{6.6\times10^{-34}\times3\times10^8}{4000\times10^{-10}\times1.6\times10^{-19}}\ \text{eV}$$

$= \frac{12400}{4000}$

$= 3.1$ eV

≈ 3 eV

7. Ans. Correct answer is 125

Explanation

Power $\mathrm{P_{zm}} = \mathrm{I_{zm}} \mathrm{V}_z$

$$\mathrm{I_{ZM}} = \frac{P_{zM}}{V_z} = \frac{0.4}{10} = 0.04\,\mathrm{A}$$

$$\text{So, } R_P = \frac{E_{\max} - V_z}{I_{ZM}} = \frac{15 - 10}{0.04} = \frac{5}{0.04} = 125\Omega$$

8. Ans. Correct answer is 14

Explanation

Conserving energy,

$\frac{1}{2}mv^2 = \frac{1}{2}m(6 \times 10^5)^2 - 0.4\,eV$

$\Rightarrow v = \sqrt{(6 \times 10^5)^2 - \frac{2 \times 1.6 \times 10^{-19} \times 0.4}{9 \times 10^{-31}}}$

$= \sqrt{36 \times 10^{10} - \frac{1.28}{9} \times 10^{12}}$

$\Rightarrow v = \frac{14}{3} \times 10^5$ m/s

$\Rightarrow x = 14$

9. Ans. Correct answer is 2

Explanation

Power gain $= \left[\frac{\Delta i_C}{\Delta i_B}\right]^2 \times \frac{R_o}{R_i}$

$= \left[\frac{10^{-2}}{10^{-4}}\right]^2 \times \frac{2}{1}$

$= 2 \times 10^4$

$\Rightarrow x = 2$

10. Ans. Correct answer is 2

Explanation

Minimum value of R_L for which the diode is shorted is $\frac{R_L}{R_L+100} \times 10 = 8 \Rightarrow R_L = 400\,\Omega$

For maximum value of R_L, current through diode is 10 mA

So $i_R = i_{R_L} + I_{ZM}$

$\frac{2}{100} = \frac{8}{R_L} + 10 \times 10^{-3}$

$10 \times 10^{-3} = \frac{8}{R_L}$

$R_L = 800\,\Omega$

So $\frac{R_{L\,\max}}{R_{L\,\min}} = 2$

11. Ans. Correct answer is 4

Explanation

D_1 : conducting

D_2 : open circuit

$i = \frac{1-0.6}{60+40} A$

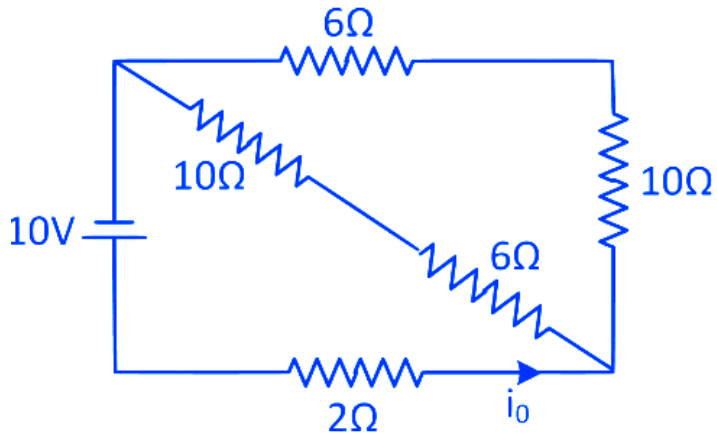
$= \frac{0.4}{100} A$

$\Rightarrow i = 4$ mA

12. Ans. Correct answer is 1

Explanation

Effective circuit will be



R_{eq} = 16 || 16 + 2 = (8 + 2) Ω

= 10 Ω

I_0 = 10 / 10

= 1 A

13. Ans. Correct answer is 15

Explanation

$$\text{Voltage gain} = \frac{I_C R_0}{I_B R_i}$$

$$= \frac{(10\ mA)(60\ \Omega)}{(200\ \mu A)(200\ \Omega)}$$

$\Rightarrow$ Voltage gain = 15

14. Ans. Correct answer is 5

Explanation

V_L = 5 V as V_Z = 5 V

$$\therefore I_L = \frac{V_L}{R_L} = \frac{5}{10^3} = 5\ \text{mA}$$

15. Ans. Correct answer is 750

Explanation

$$R_B = \frac{10\times10^{-3}}{10\times10^{-6}}$$

$$= 10^3\,\Omega$$

$$\therefore A_v = \left(\frac{\Delta I_C}{\Delta I_B}\right) \times \left(\frac{R_C}{R_B}\right)$$

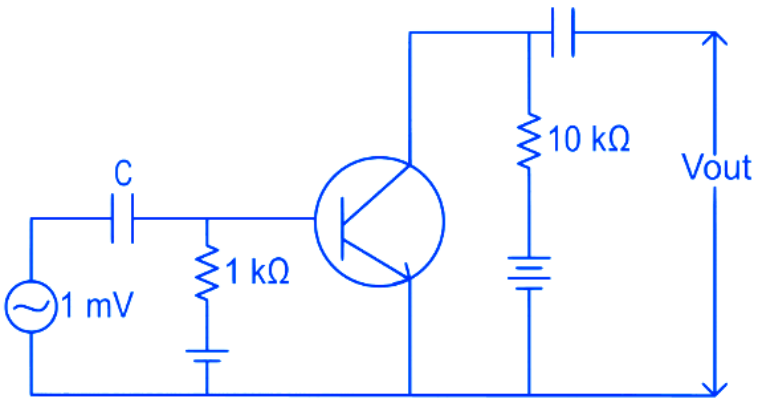
$$= \frac{1.5\times10^{-3}}{10\times10^{-6}} \times \frac{5\times10^3}{1\times10^3}$$

$$= \frac{1.5\times5}{10} \times (1000)$$

$$= 750$$

MCQ (Single Correct Answer)

Q.1. An n.p.n transistor with current gain β=100 in common emitter configuration is shown in figure. The output voltage of the amplifier will be



A 0.1 V

B 1.0 V

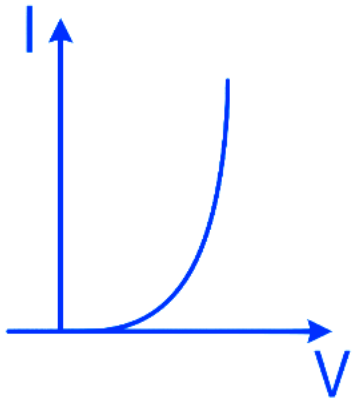
C 10 V

D 100 V

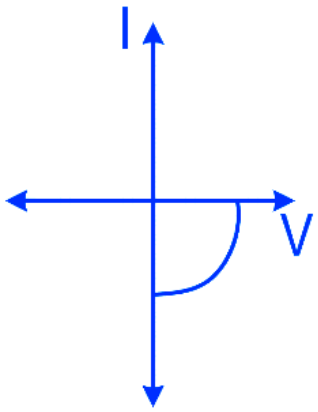
JEE Main 2022 (Online) 28th July Evening Shift

Q.2. Identify the solar cell characteristics from the following options :

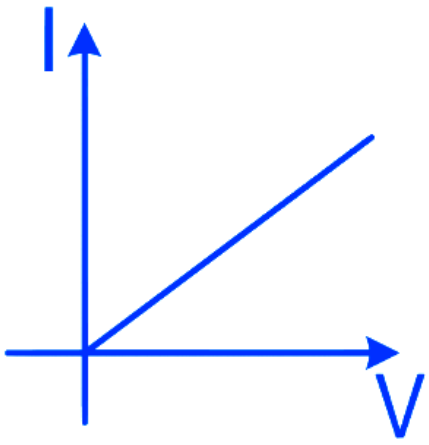
A



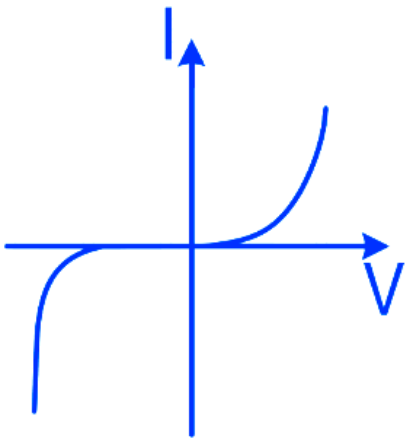
B



C



D



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Q.3. For a constant collector-emitter voltage of 8 V, the collector current of a transistor reached to the value of 6 mA from 4 mA, whereas base current changed from 20μA to 25μA value. If transistor is in active state, small signal current gain (current amplification factor) will be :

A 240

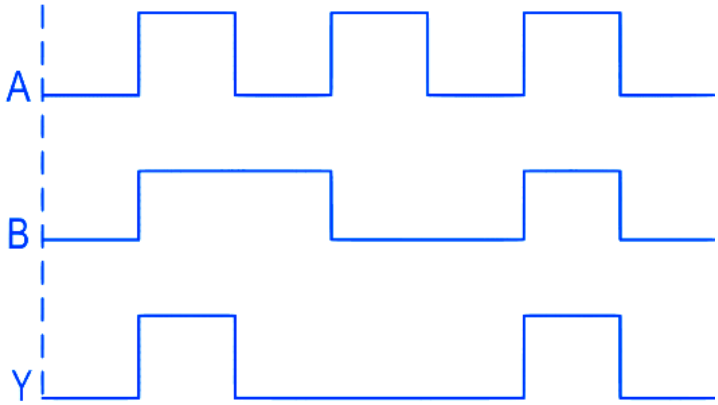
B 400

C 0.0025

D 200

JEE Main 2022 (Online) 27th July Evening Shift

Q.4. A logic gate circuit has two inputs A and B and output Y. The voltage waveforms of A, B and Y are shown below.



The logic gate circuit is :

A AND gate

B OR gate

C NOR gate

D NAND gate

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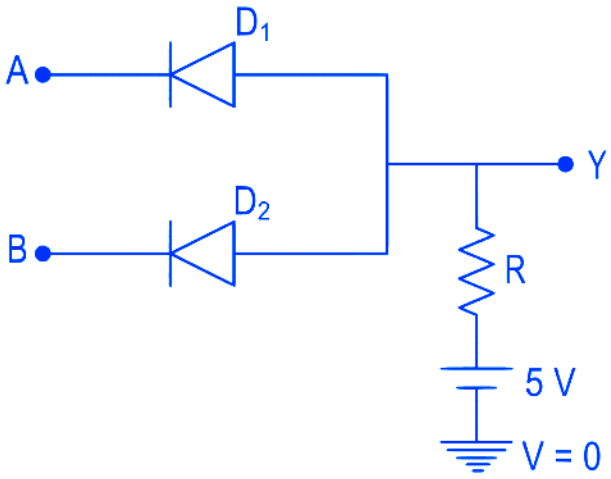
Q.5. In the circuit, the logical value of A=1 or B=1 when potential at A or B is 5 V and the logical value of A=0 or B=0 when potential at A or B is 0 V.



The truth table of the given circuit will be :

A

A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

B

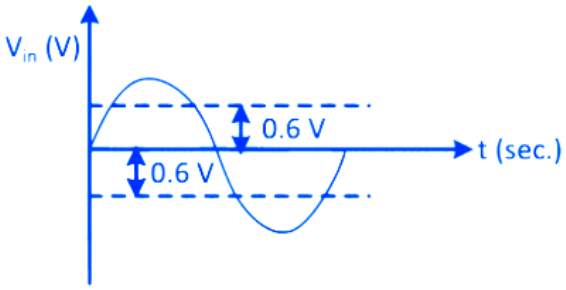
A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

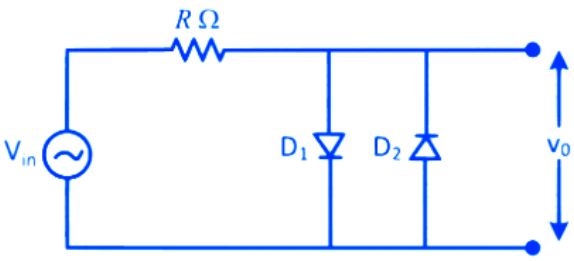
	A	B	Y
	0	0	0
C	1	0	0
	0	1	0
	1	1	0

	A	B	Y
	0	0	1
D	1	0	1
	0	1	1
	1	1	0

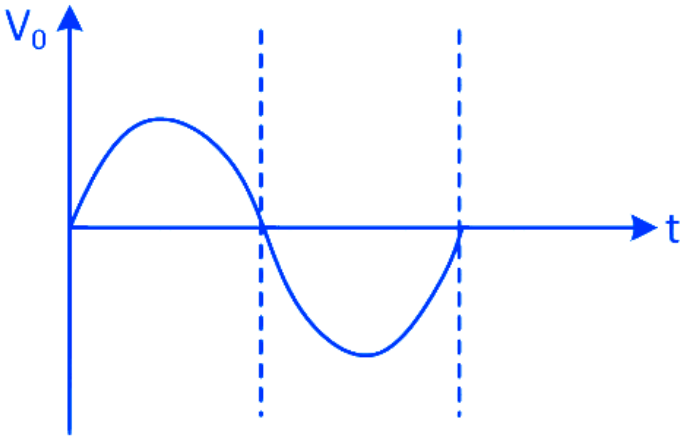
JEE Main 2022 (Online) 25th July Morning Shift

Q.6. In the given circuit the input voltage V_{in} is shown in figure. The cut-in voltage of p-n junction diode (D_1 or D_2) is 0.6 V. Which of the following output voltage (V_0) waveform across the diode is correct?

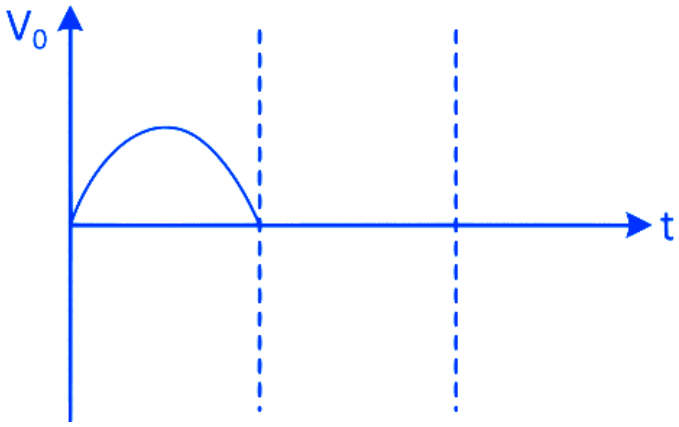




A



B



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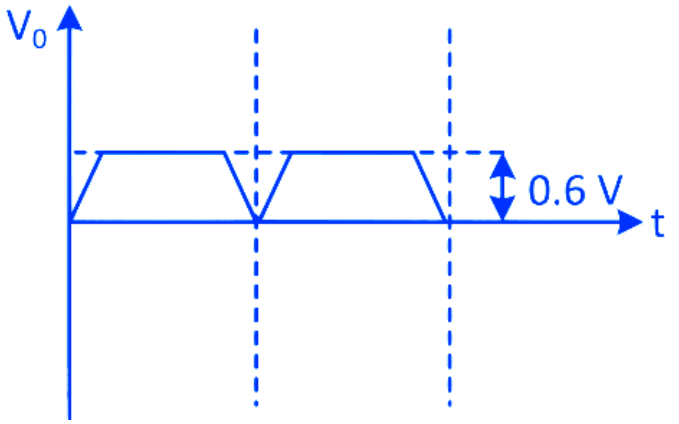
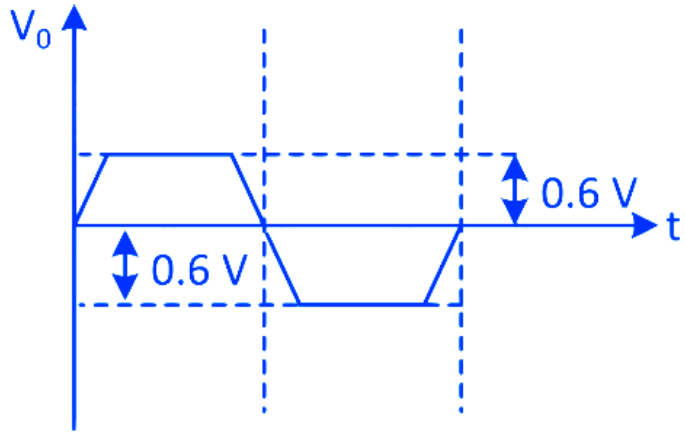
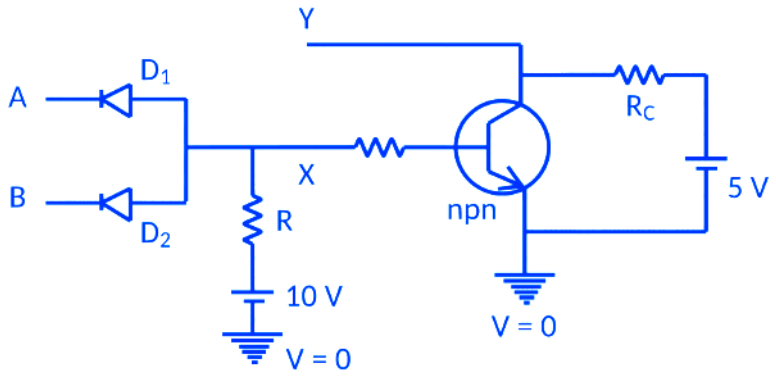


D



JEE Main 2022 (Online) 28th June Evening Shift

Q.7. In the following circuit, the correct relation between output (Y) and inputs A and B will be :



A Y = AB

B Y = A + B

C $Y = \overline{AB}$

D $Y = \overline{A + B}$

JEE Main 2022 (Online) 28th June Morning Shift

Q.8. For using a multimeter to identify diode from electrical components, choose the correct statement out of the following about the diode :

A It is two terminal device which conducts current in both directions.

B It is two terminal device which conducts current in one direction only.

C It does not conduct current gives an initial deflection which decays to zero.

D It is three terminal device which conducts current in one direction only between central terminal and either of the remaining two terminals

JEE Main 2022 (Online) 28th June Morning Shift

Q.9. Given below are two statements : One is labelled as Assertion A and the other is labelled as Reason R.

Assertion A : n-p-n transistor permits more current than a p-n-p transistor.

Reason R : Electrons have greater mobility as a charge carrier.

Choose the correct answer from the options given below :

A Both A and R are true, and R is correct explanation of A.

B Both A and R are true but R is NOT the correct explanation of A.

C A is true but R is false.

D A is false but R is true.

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Q.10. For a transistor to act as a switch, it must be operated in

A Active region.

B Saturation state only.

C Cut-off state only.

D Saturation and cut-off state.

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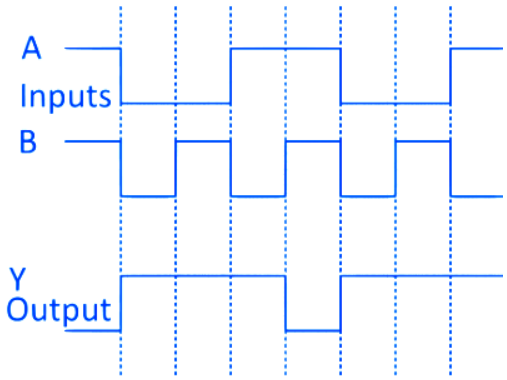
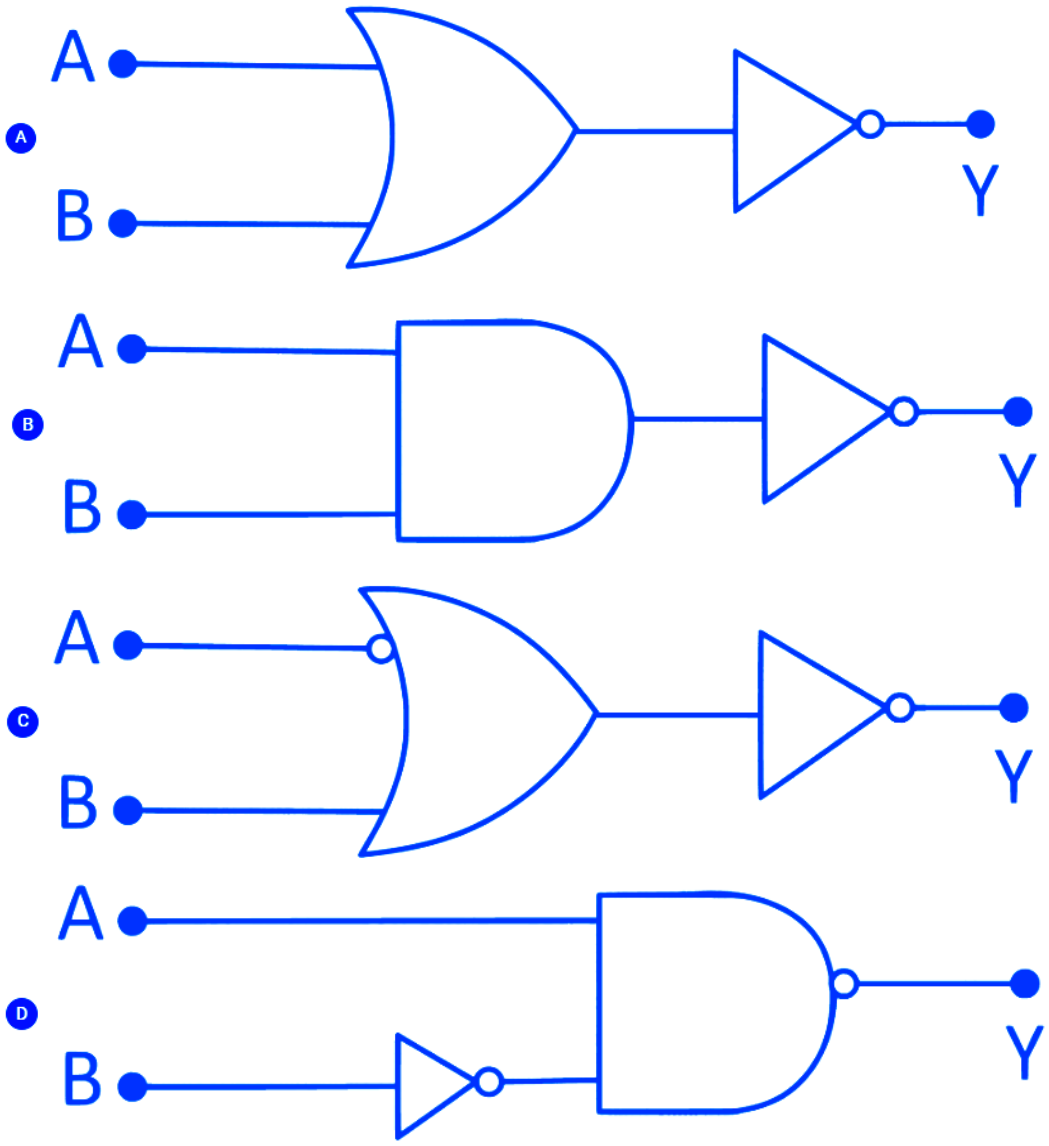
Q.11. Identify the correct Logic Gate for the following output (Y) of two inputs A and B.





JEE Main 2022 (Online) 27th June Morning Shift

Q.12. The positive feedback is required by an amplifier to act an oscillator. The feedback here means :

A External input is necessary to sustain ac signal in output.

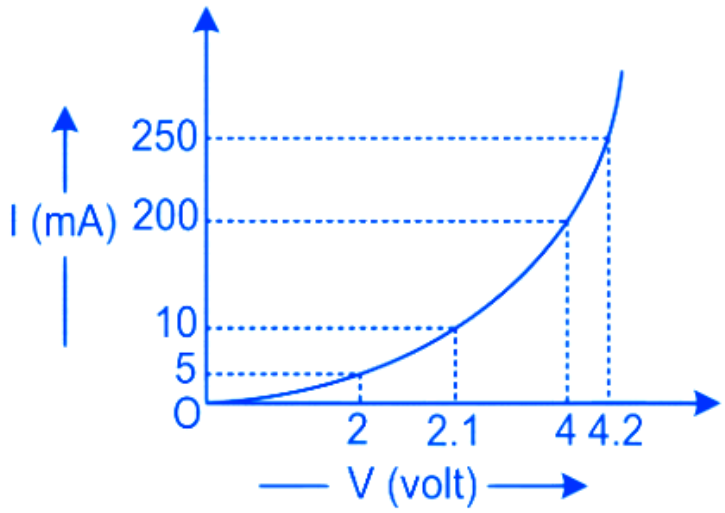
B A portion of the output power is returned back to the input.

C Feedback can be achieved by LR network.

D The base-collector junction must be forward biased.

JEE Main 2022 (Online) 26th June Evening Shift

Q.13. The I-V characteristics of a p-n junction diode in forward bias is shown in the figure. The ratio of dynamic resistance, corresponding to forward bias voltage of 2 V and 4 V respectively, is :



A 1 : 2

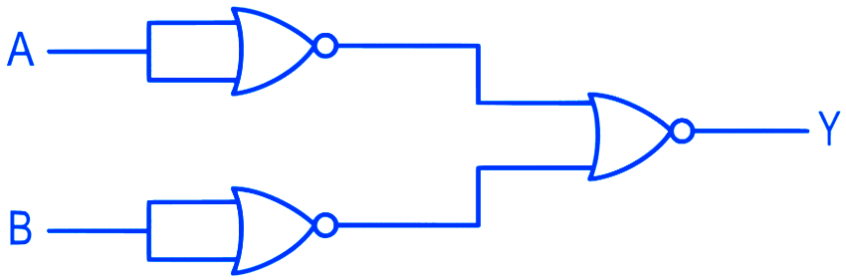
B 5 : 1

C 1 : 40

D 20 : 1

JEE Main 2022 (Online) 26th June Morning Shift

Q.14. Identify the logic operation performed by the given circuit:



A AND gate

B OR gate

C NOR gate

D NAND gate

JEE Main 2022 (Online) 25th June Evening Shift

Q.15. The photodiode is used to detect the optical signals. These diodes are preferably operated in reverse biased mode because :

A fractional change in majority carriers produce higher forward bias current

B fractional change in majority carriers produce higher reverse bias current

C fractional change in minority carriers produce higher forward bias current

D fractional change in minority carriers produce higher reverse bias current

JEE Main 2022 (Online) 25th June Morning Shift

Answer key & Explanation

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1. Ans. (B)

Explanation

$$\frac{V_0}{V_i} = \beta \times \left(\frac{R_C}{R_B}\right)$$

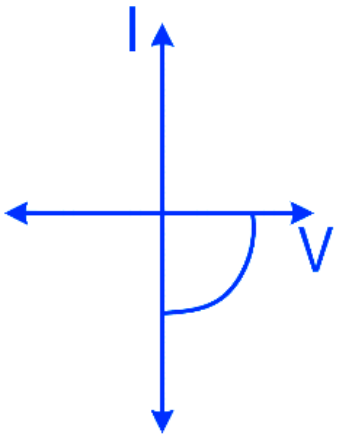
$$\Rightarrow V_0 = 100 \times \left(\frac{10}{1}\right) \times 10^{-3}$$

$$= 1.0\,\text{V}$$

2. Ans. (B)

Explanation

Solar cell characteristics



3. Ans. (B)

Explanation

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

$$= \frac{(6-4)\times 10^{-3}}{(25-20)\times 10^{-6}}$$

$$= \frac{2}{5} \times 10^3$$

$$= 400$$

4. Ans. (A)

Explanation

From waveforms, it is an AND gate.

5. Ans. (A)

Explanation

Given circuit is equivalent to an AND gate.

	A	B	Y
	0	0	0
$\therefore$	0	1	0
	1	0	0
	1	1	1

6. Ans. (D)

Explanation

Till $|V| \leq 0.6V$

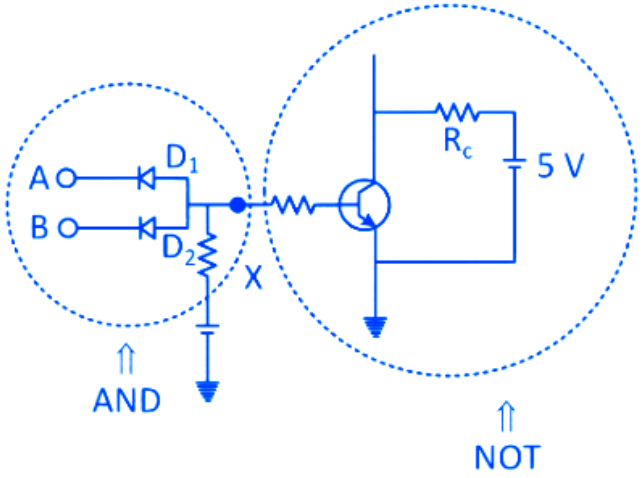
$|V_0| = |V|$

So correct graph will be D.

7. Ans. (C)

Explanation

The shown circuit is a combination of AND gate and a NOT gate



$\Rightarrow Y = \overline{AB}$

8. Ans. (B)

Explanation

A diode is a two terminal device which conducts current in forward bias only.

9. Ans. (A)

Explanation

(A) is true as n-p-n transistor permits more current than p-n-p transistor as electrons which are majority charge carriers in n-p-n have higher mobility than holes which are majority carriers in p-n-p transistor.

⇒ Statement R is correct explanation of statement A.

10. Ans. (D)

Explanation

A transistor acts as a switch when it is operated in saturation and cut-off state.

11. Ans. (B)

Explanation

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$\Rightarrow$ Y = (AB)' $\Rightarrow$

12. Ans. (B)

Explanation

Feedback means a portion of the output power is fed to the inputs.

13. Ans. (B)

Explanation

$\therefore R = \frac{\Delta v}{\Delta i}$

Now, dynamic resistance at $V = 2V$ is

$R_2 = \frac{0.1}{5 \times 10^{-3}}\ \Omega$

= 20 Ω

Similarly,

$R_4 = \frac{0.2}{50 \times 10^{-3}} = 4\,\Omega$

$\frac{R_2}{R_4} = \frac{5}{1}$

14. Ans. (A)

Explanation

According to the circuit,

$Y = (A' + B')'$

$\Rightarrow Y = AB$

$\Rightarrow$ AND gate

15. Ans. (D)

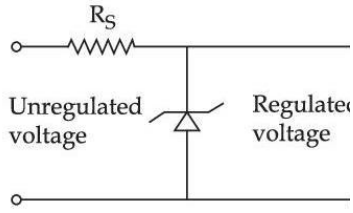
Explanation

A photodiode is reverse biased. When light falling on it produces charge carriers, the fractional change, in minority carriers is high since the original current is very small.x

2021

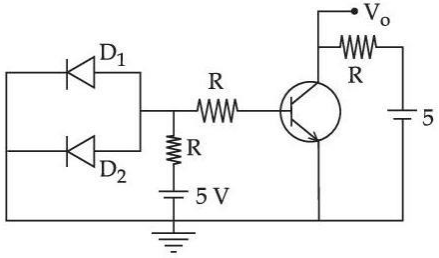
Numerical

Q.1 A zener diode of power rating 2W is to be used as a voltage regulator. If the zener diode has a breakdown of 10 V and it has to regulate voltage fluctuated between 6 V and 14 V, the value of R_s for safe operation should be _____ Ω.



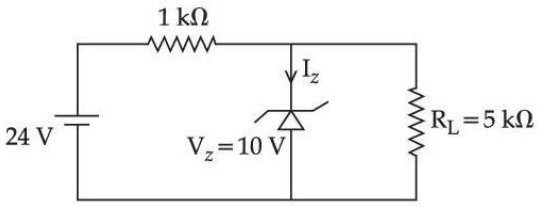
27th Aug Evening Shift 2021

Q.2 A circuit is arranged as shown in figure. The output voltage V_0 is equal to ..... V.



27th Aug Morning Shift 2021

Q.3 For the given circuit, the power across Zener diode is ..... mW.



26th Aug Evening Shift 2021

Q.4 If the maximum value of accelerating potential provided by a ratio frequency oscillator is 12 kV. The number of revolution made by a proton in a cyclotron to achieve one sixth of the speed of light is .....

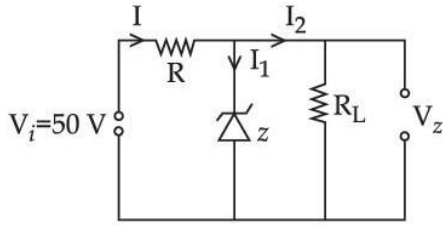
[$m_p = 1.67 \times 10^{-27}$ kg, e = 1.6 ×× 10^{-19}C, Speed of light = 3×10^8 m/s]

26th Aug Evening Shift 2021

Q.5 In a semiconductor, the number density of intrinsic charge carries at 27°C is $1.5 \times 10^{16}/m^3$. If the semiconductor is doped with impurity atom, the hole density increases to $4.5 \times 10^{22}/m^3$. The electron density in the doped semiconductor is _____ $\times 10^9/m^3$.

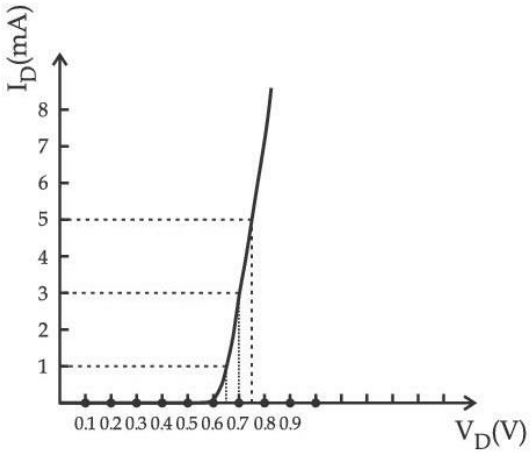
25th July Evening Shift 2021

Q.6 In a given circuit diagram, a 5 V zener diode along with a series resistance is connected across a 50 V power supply. The minimum value of the resistance required, if the maximum zener current is 90 mA will be _____ Ω.



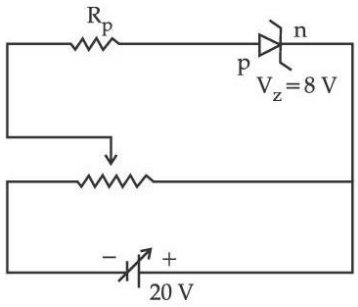
22th July Evening Shift 2021

Q.7 For the forward biased diode characteristics shown in the figure, the dynamic resistance at I_D = 3 mA will be _____ Ω.



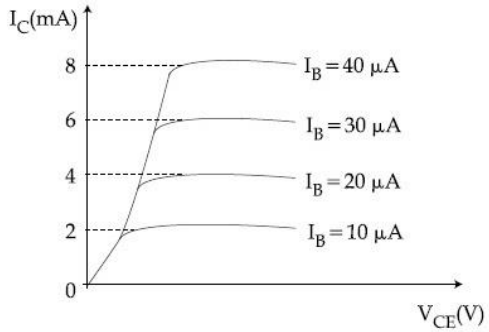
20th July Evening Shift 2021

Q.8 A zener diode having zener voltage 8 V and power dissipation rating of 0.5 W is connected across a potential divider arranged with maximum potential drop across zener diode is as shown in the diagram. The value of protective resistance R_p is ..... Ω.



20th July Evening Shift 2021

Q.9 The typical output characteristics curve for a transistor working in the common-emitter configuration is shown in the figure.



The estimated current gain from the figure is _____.

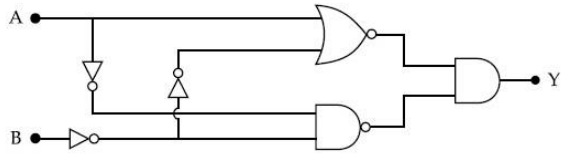
18th Mar Evening Shift 2021

Q.10 An npn transistor operates as a common emitter amplifier with a power gain of 10^6. The input circuit resistance is 100Ω and the output load resistance is 10 KΩ. The common emitter current gain 'β' will be _____. (Round off to the Nearest Integer).

18th Mar Morning Shift 2021

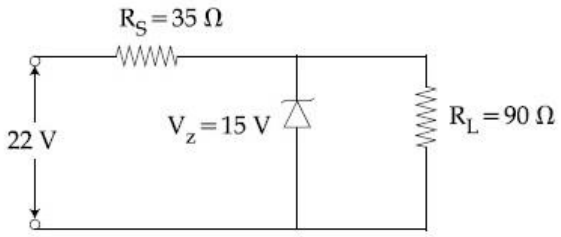
Q.11 In the logic circuit shown in the figure, if input A and B are 0 to 1 respectively, the output at Y would be 'x'.

The value of x is _____.



16th Mar Morning Shift 2021

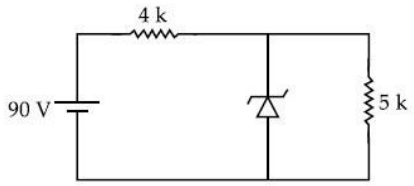
Q.12 The value of power dissipated across the zener diode (V_z = 15V) connected in the circuit as shown in the figure is x × 10^{-1} watt.



The value of x, to the nearest integer, is _____.

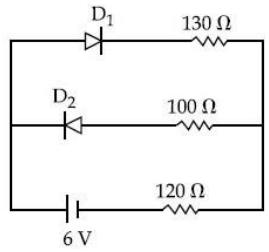
16th Mar Morning Shift 2021

Q.13 The zener diode has a V_z = 30V. The current passing through the diode for the following circuit is _____ mA.



26th Feb Evening Shift 2021

Q.14 The circuit contains two diodes each with a forward resistance of 50Ω and with infinite reverse resistance. If the battery voltage is 6V, the current through the 120Ω resistance is _____ mA.



26th Feb Morning Shift 2021

Numerical Answer Key

1. **Ans. (20)**
2. **Ans. (5)**
3. **Ans. (120)**
4. **Ans. (543)**
5. **Ans. (5)**
6. **Ans. (500)**
7. **Ans. (25)**
8. **Ans. (192)**
9. **Ans. (200)**
10. **Ans. (100)**
11. **Ans. (0)**
12. **Ans. (5)**
13. **Ans. (9)**
14. **Ans. (20)**

Numerical Explanation

Ans 1. When unregulated voltage is 14 V voltage across zener diode must be 10 V.
So potential difference across resistor $\Delta V_{Rs} = 4V$

and $P_{zener} = 2W$

$VI = 2$

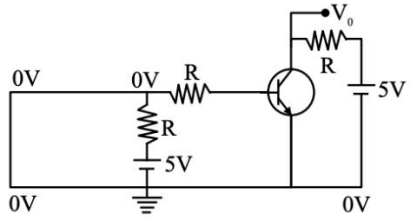
$I = \frac{2}{10} = 0.2\ A$

$\Delta V_{Rs} = I\ R_s$

$4 \times 0.2\ R_s \Rightarrow R_s = \frac{40}{2} = 20\Omega$

Ans 2. As diodes D_1 and D_2 are in forward bias, so they acted as negligible resistances

⇒ Input voltage become zero

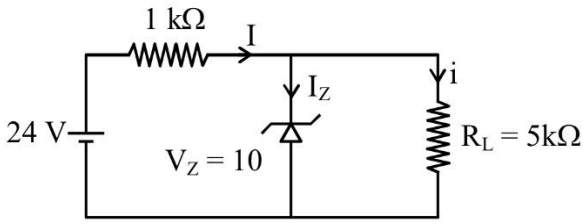


⇒ Input current is zero

⇒ Output current is zero

⇒ $V_0 = 5$ volt

Ans 3.



$i = \frac{10V}{5k\Omega} = 2mA$

$I = \frac{14V}{1k\Omega} = 14\ mA$

∴ $I_z = 12$ mA

∴ $P = I_z V_z = 120$ mW

Ans 4. V = 12 kV

Number of revolution = n

$$n[2 \times q_P \times V] = \frac{1}{2} m_P \times v_P^2$$

$$n[2 \times 1.6 \times 10^{-19} \times 12 \times 10^3]$$

$$= \frac{1}{2} \times 1.67 \times 10^{-27} \times \left[\frac{3 \times 10^8}{6}\right]^2$$

$n(38.4 \times 10^{-16}) = 0.2087 \times 10^{-11}$

$n = 543.4$

Ans 5.

$$n_e n_h = {n_i}^2$$

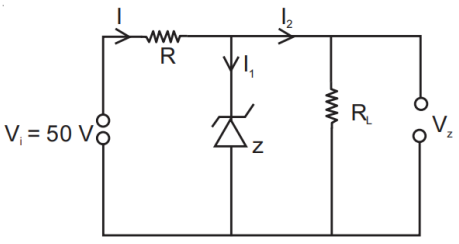
$$n_e = \frac{{n_i}^2}{n_h} = \frac{(1.5 \times 10^{16})^2}{4.5 \times 10^{22}}$$

$$= \frac{1.5 \times 1.5 \times 10^{32}}{4.5 \times 10^{22}}$$

$$= 5 \times 10^9/\text{m}^3$$

Ans 6.

$$I = \frac{50 - V_z}{R} = \frac{5}{R_L} + 90 \times 10^{-3}$$



For $R_L \to \infty$

$R = 500\Omega$

Ans 7.

$$R_d = \frac{dV}{di} = \frac{1}{\frac{di}{dv}} = \frac{1}{\frac{5-1\times10^{-3}}{0.75-0.65}}$$

$$= \frac{100}{4} = 25\Omega$$

Ans 8.

P = Vi

0.5 = 8i

$i = \frac{1}{16}A$

E = 20 = 8 + i R_p

R_p = 12 ×× 16 = 192Ω

Ans 9. For common emitter configuration

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{(4-2)\,mA}{(20-10)\,\mu A}$$

$$= \frac{2}{10} \times \frac{10^{-3}}{10^{-6}} = 200$$

Ans 10.

Power gain = 10^6

Input resistance = 100Ω

Output load resistance = 10KΩ

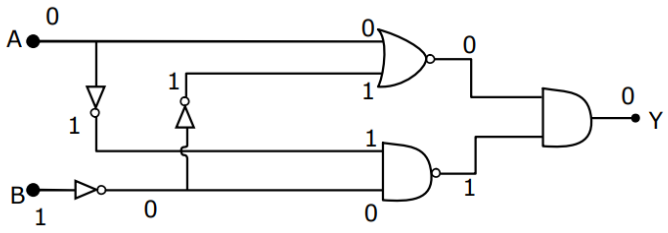
$$\text{Power gain} = \beta^2 \times \frac{r_{out}}{R_{in}}$$

$$\Rightarrow 10^6 = \beta^2 \times \frac{10\times10^3}{100}$$

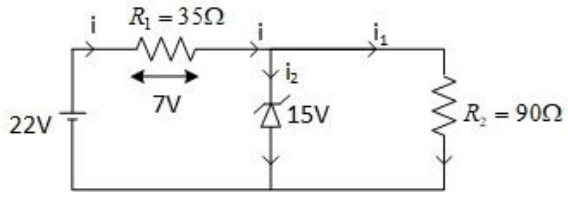
⇒ $\beta^2 = 10^4$

⇒ β = 100

Ans 11.



Ans 12.



$$i = \frac{7}{35} = \frac{1}{5}A$$

$$i_1 = \frac{15}{90} = \frac{1}{6}A$$

$$i_2 = i - i_1$$

$$i_2 = \frac{1}{5} - \frac{1}{6}$$

$$i_2 = \frac{1}{30}A$$

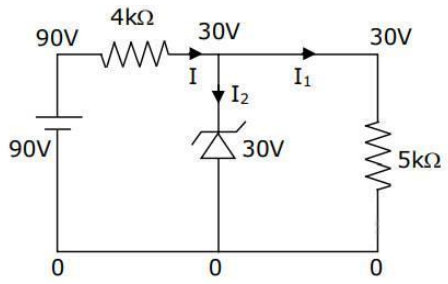
Power across diode; $P = V_2\, i_2$

$$P = 15 \times \frac{1}{30}$$

$$P = 0.5\ W$$

$$\therefore P = 5 \times 10^{-1}\ W$$

Ans 13.



$$I = \frac{90-30}{4} = 15mA$$

$$I_1 = \frac{30}{5K\Omega} = 6mA$$

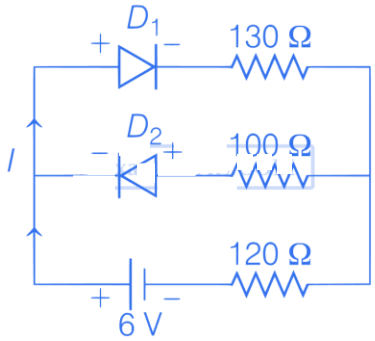
$$I_2 = 15mA - 6mA = 9mA$$

Ans 14. Given, forward resistance, $R_1 = 50\ \Omega$

Reverse resistance, R_2 = infinity

Battery voltage = 6V

According to circuit diagram,



In this case, diode D_1 is forward biased, whereas diode D_2 is reverse biased.

So, D_2 will act as open circuit.

$$6 - 50I - 130I - 120I = 0$$

$$\Rightarrow 6 = 300I$$

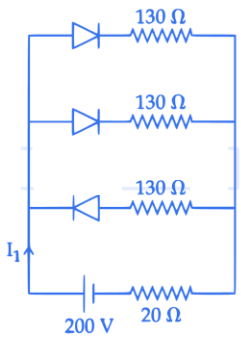
$$\Rightarrow I = \frac{6}{300} = \frac{1}{50}$$

$$= \frac{2}{100} = 0.02 \text{ A} = 20 \text{ mA}$$

Hence, current through 120 Ω = 20 mA

MCQ (Single Correct Answer)

Q.1 In the given figure, each diode has a forward bias resistance of 30ΩΩ and infinite resistance in reverse bias. The current I_1 will be :



A 3.75 A

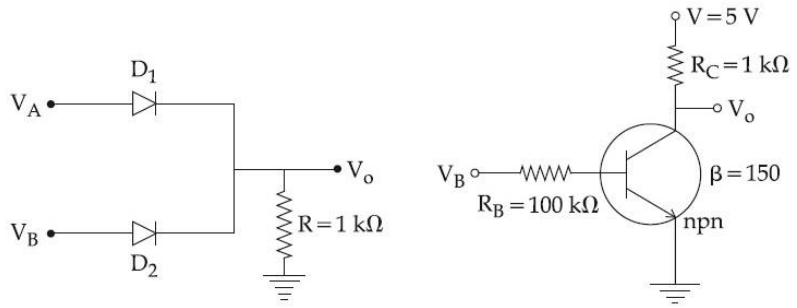
B 2.35 A

C 2 A

D 2.73 A

1st Sep Evening Shift 2021

Q.2 If V_A and V_B are the input voltages (either 5V or 0V) and V_0 is the output voltage then the two gates represented in the following circuit (A) and (B) are :-



(A) (B)

A AND and OR Gate

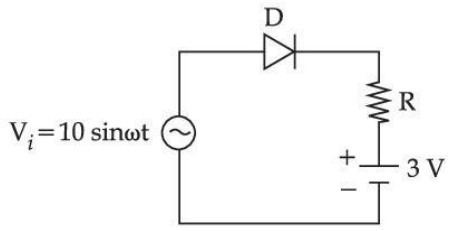
B OR and NOT Gate

C NAND and NOR Gate

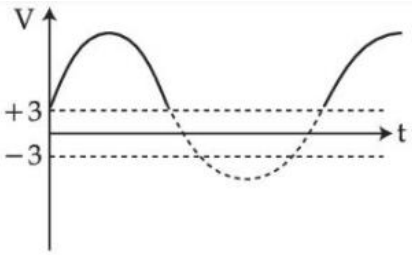
D AND and NOT Gate

31st Aug Evening Shift 2021

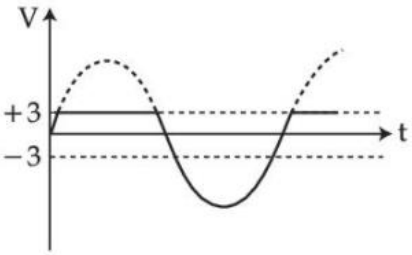
Q.3 Choose the correct waveform that can represent the voltage across R of the following circuit, assuming the diode is ideal one :



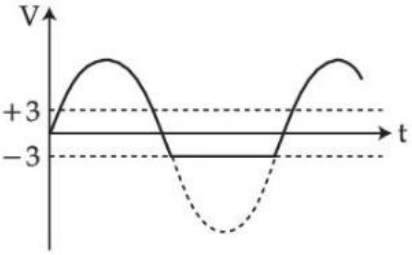
A



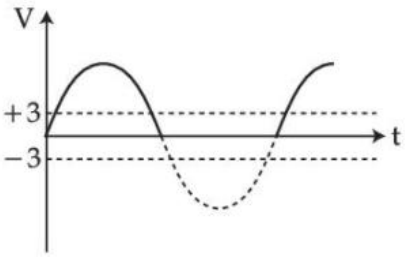
B



C

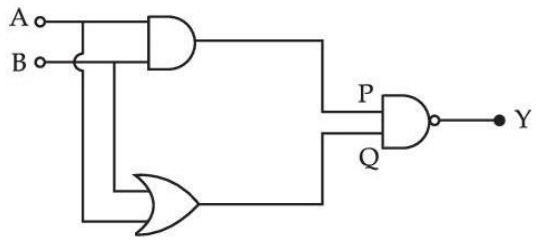


D



31st Aug Morning Shift 2021

Q.4 In the following logic circuit the sequence of the inputs A, B are (0, 0), (0, 1), (1, 0) and (1, 1). The output Y for this sequence will be :



A 1, 0, 1, 0

B 0, 1, 0, 1

C 1, 1, 1, 0

D 0, 0, 1, 1

31st Aug Morning Shift 2021

Q.5 For a transistor α and β are given as $\alpha = \frac{I_C}{I_E}$ and $\beta = \frac{I_C}{I_B}$. Then the correct relation between α and β will be :

A $\alpha = \frac{1-\beta}{\beta}$

B $\beta = \frac{\alpha}{1-\alpha}$

C $\alpha\beta = 1$

D $\alpha = \frac{\beta}{1-\beta}$

27th Aug Evening Shift 2021

Q.6 For a transistor in CE mode to be used as an amplifier, it must be operated in :

(A) Both cut-off and Saturation

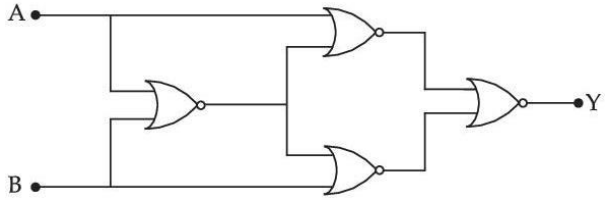
(B) Saturation region only

(C) Cut-off region only

(D) The active region only

27th Aug Morning Shift 2021

Q.7 Four NOR gates are connected as shown in figure. The truth table for the given figure is :



(A)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

(B)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(C)

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1

(D)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

26th Aug Evening Shift 2021

Q.8 Statement I : By doping silicon semiconductor with pentavalent material, the electrons density increases.

Statement II : The n-type semiconductor has net negative charge.

In the light of the above statements, choose the most appropriate answer from the options given below :

(A) Statement - I is true but Statement - II is false.

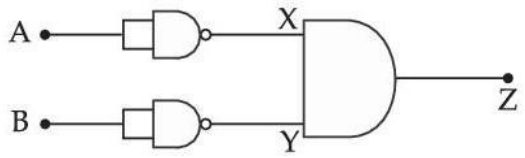
(B) Statement - I is false but Statement - II is true.

(C) Both Statement I and Statement II are true.

(D) Both Statement I and Statement II are false.

26th Aug Morning Shift 2021

Q.9 Identify the logic operation carried out by the given circuit :-



A OR

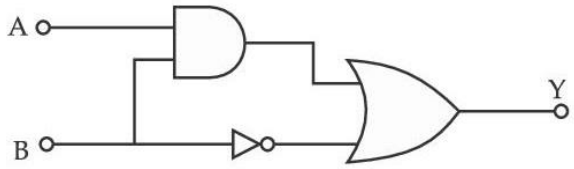
B AND

C NOR

D NAND

26th Aug Morning Shift 2021

Q.10 Find the truth table for the function Y of A and B represented in the following figure.



A

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	0

B

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

C

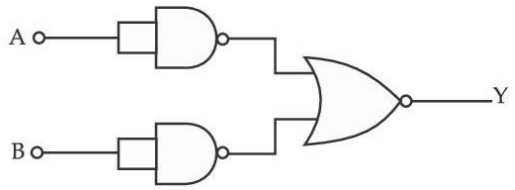
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

D

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

27th July Evening Shift 2021

Q.11 Identify the logic operation carried out.



A OR

B AND

C NOR

D NAND

25th July Morning Shift 2021

Q.12 Consider a situation in which reserve biased current of a particular P-N junction increases when it is exposed to a light of wavelength ≤ 621 nm. During this process, enhancement in carrier concentration takes place due to generation of hole-electron pairs. The value of band gap is nearly.

A 1 eV

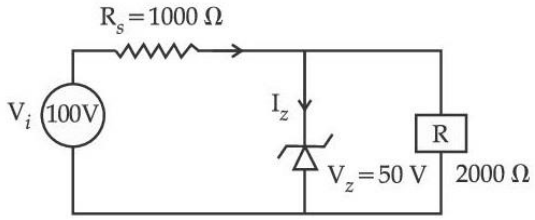
B 4 eV

C 0.5 eV

D 2 eV

22th July Evening Shift 2021

Q.13 For the circuit shown below, calculate the value of I_z :



A 25 mA

B 0.1 A

C 0.15 A

D 0.05 A

20th July Morning Shift 2021

Q.14 The correct relation between α (ratio of collector current to emitter current) and β (ratio of collector current to base current) of a transistor is :

A $\beta = \frac{\alpha}{1+\alpha}$

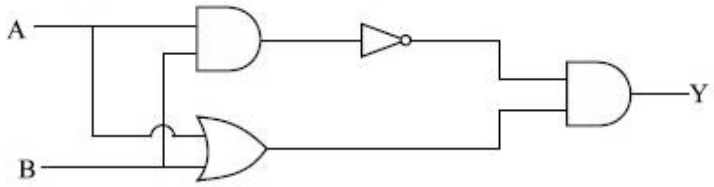
B $\alpha = \frac{\beta}{1-\alpha}$

C $\alpha = \frac{\beta}{1+\beta}$

D $\beta = \frac{1}{1-\alpha}$

18th Mar Evening Shift 2021

Q.15 Which one of the following will be the output of the given circuit?



A XOR Gate

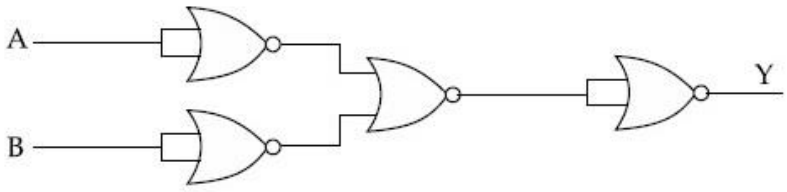
B NOR Gate

C NAND Gate

D AND Gate

17th Mar Evening Shift 2021

Q.16 The output of the given combination gates represents :



A AND Gate

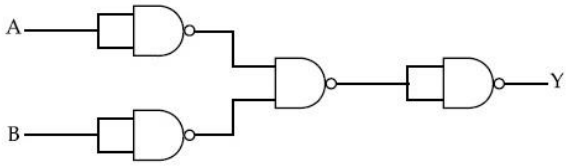
B NOR Gate

C NAND Gate

D XOR Gate

17th Mar Morning Shift 2021

Q.17 The following logic gate is equivalent to :



A NOR Gate

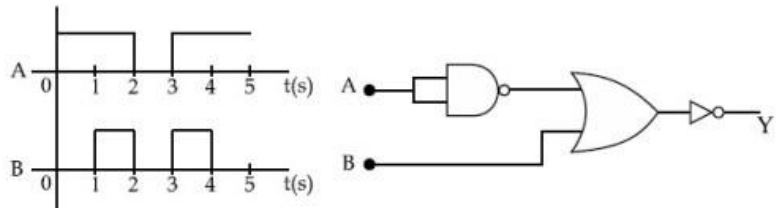
B NAND Gate

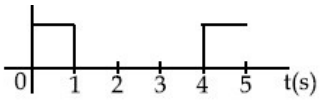
C OR Gate

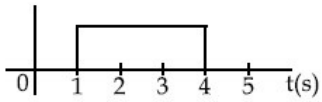
D AND Gate

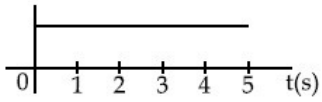
16th Mar Evening Shift 2021

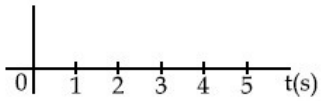
Q.18 Draw the output signal Y in the given combination of gates.



A 

B 

C 

D 

26th Feb Evening Shift 2021

Q.19 LED is constructed from Ga-As-P semiconducting material. The energy gap of this LED is 1.9 eV. Calculate the wavelength of light emitted and its colour.

[h = 6.63×10^{-34} Js and c = $3 \times\times 10^{8}$ ms^{-1}]

A 654 nm and orange colour

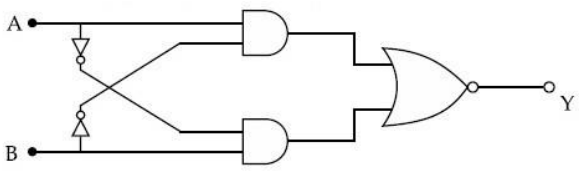
B 654 nm and red colour

C 1046 nm and red colour

D 1046 nm and blue colour

26th Feb Morning Shift 2021

Q.20 The truth table for the following logic circuit is :



A

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

B

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

C

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1

D

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

26th Feb Evening Shift 2021

Q.21 For extrinsic semiconductors; when doping level is increased;

A Fermi-level of both p-type and n-type semiconductors will go upward for $T > T_F K$ and downward for $T < T_F K$, where T_F is Fermi temperature.

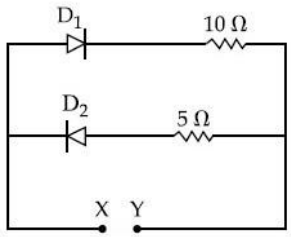
B Fermi-level of p-type semiconductor will go upward and Fermi-level of n-type semiconductors will go downward

C Fermi-level of p and n-type semiconductors will not be affected.

D Fermi-level of p-type semiconductors will go downward and Fermi-level of n-type semiconductor will go upward.

25th Feb Evening Shift 2021

Q.22 A 5V battery is connected across the points X and Y. Assume D_1 and D_2 to be normal silicon diodes. Find the current supplied by the battery if the +ve terminal of the battery is connected to point X.



A ~ 0.5 A

B ~ 1.5 A

C ~ 0.43 A

D ~ 0.86 A

25th Feb Morning Shift 2021

Q.23 Zener breakdown occurs in a p – n junction having p and n both :

A heavily doped and have wide depletion layer.

B lightly doped and have narrow depletion layer.

C heavily doped and have narrow depletion layer.

D lightly doped and have wide depletion layer.

24th Feb Evening Shift 2021

Q.24 Given below are two statements :

Statement I : PN junction diodes can be used to function as transistor, simply by connecting two diodes, back to back, which acts as the base terminal.

Statement II : In the study of transistor, the amplification factor ββ indicates ratio of the collector current to the base current.

In the light of the above statements, choose the correct answer from the options given below.

A Both Statement I and Statement II are false

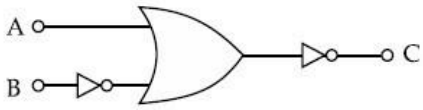
B Statement I is false but Statement II is true

C Both Statement I and Statement II are true

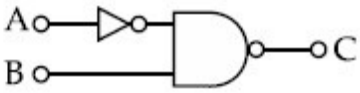
D Statement I is true but Statement II is false

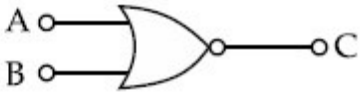
24th Feb Evening Shift 2021

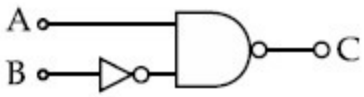
Q.25

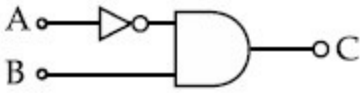


The logic circuit shown above is equivalent to :

A 

B 

C 

D 

24th Feb Evening Shift 2021

Q.26 If an emitter current is changed by 4 mA, the collector current changes by 3.5 mA. The value of β will be:

A 0.875

B 0.5

C 3.5

D 7

24th Feb Morning Shift 2021

MCQ Answer Key

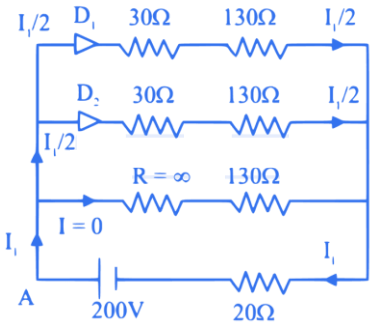
1. Ans.(c)	10. Ans.(b)	19. Ans.(b)
2. Ans.(b)	11. Ans.(b)	20. Ans.(d)
3. Ans.(d)	12. Ans.(d)	21. Ans.(d)
4. Ans.(c)	13. Ans.(a)	22. Ans.(c)
5. Ans.(b)	14. Ans.(c)	23. Ans.(c)
6. Ans.(d)	15. Ans.(a)	24. Ans.(b)
7. Ans.(d)	16. Ans.(c)	25. Ans.(d)
8. Ans.(a)	17. Ans.(a)	26. Ans.(d)
9. Ans.(c)	18. Ans.(a)	

MCQ Explanation

Ans 1. As per diagram,

Diode D_1 & D_2 are in forward bias i.e. R = 30Ω whereas diode D_3 is in reverse bias i.e. R = infinite ⇒ Equivalent circuit will be

Applying KVL starting from point A



$$-\left(\frac{I_1}{2}\right)\times 30-\left(\frac{I_1}{2}\right)\times 130-I_1\times 20+200=0$$

⇒ $-100\ I_1 + 200 = 0$

$I_1 = 2$

Ans 2.

$V_A = 5V \Rightarrow A = 1$

$V_A = 0V \Rightarrow A = 0$

$V_B = 5V \Rightarrow B = 1$

$V_B = 0V \Rightarrow B = 0$

If A = B = 0, there is no potential anywhere here $V_0 = 0$

If A = 1, B = 0, Diode D_1 is forward biased, here $V_0 = 5V$

If A = 0, B = 1, Diode D_2 is forward biased hence $V_0 = 5V$

If A = 1, B = 1, Both diodes are forward biased hence $V_0 = 5V$

Truth table for Ist

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

∴ Given circuit is OR gate

For IInd circuit

$V_B = 5V$, A = 1

$V_B = 0V$, A = 0

When A = 0, E - B junction is unbiased there is no current through it

∴ $V_0 = 1$

When A = 1, E-B junction is forward biased

$V_0 = 0$

∴ Hence this circuit is NOT gate

Ans 3.

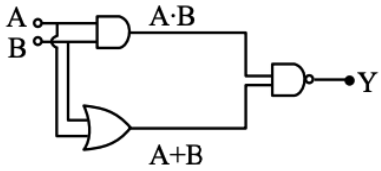
When $V_i > 3$ volt, $V_R > 0$

Because diode will be in forward biased state

When $V_i \leq 3$ volt ; $V_R = 0$

Because diode will be in reverse biased state.

Ans 4.



$$Y = \overline{(A.\ B).\ (A+B)}$$

$$Y)_{(0,0)} = 1$$

$$Y)_{(0,1)} = 1$$

$$Y)_{(1,0)} = 1$$

$$Y)_{(1,1)} = 0$$

Ans 5.

$$\alpha = \frac{I_C}{I_E},\ \beta = \frac{I_C}{I_B};\ I_E = I_C + I_B$$

$$\alpha = \frac{I_C}{I_C + I_B} = \frac{I_C/I_B}{\frac{I_C}{I_B}+1} = \frac{\beta}{\beta+1}$$

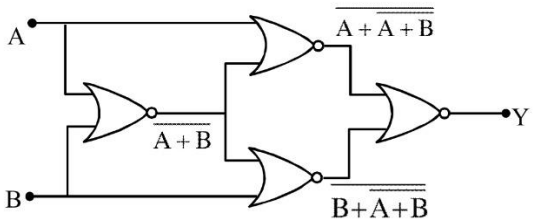
$$1 + \frac{1}{\beta} = \frac{1}{\alpha}$$

$$\frac{1}{\beta} = \frac{1-\alpha}{\alpha}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

Ans 6. Active region of the CE transistor is linear region and is best suited for its use as an amplifier.

Ans 7.



$$y = \overline{\overline{(A+\overline{\overline{A+B}})} + \overline{(B+\overline{\overline{A+B}})}}$$

$$y = (A+\overline{\overline{A+B}}).(B+\overline{\overline{A+B}})$$

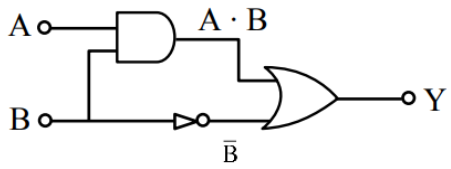
A	B	y
0	0	1
0	1	0
1	0	0
1	1	1

Ans 8. Pentavalent activities have excess free e^-, so e^- density increases but overall semiconductor is neutral.

Ans 9.

A	B	X	Y	Z
1	1	0	0	0
1	0	0	1	0
0	1	1	0	0
0	0	1	1	1

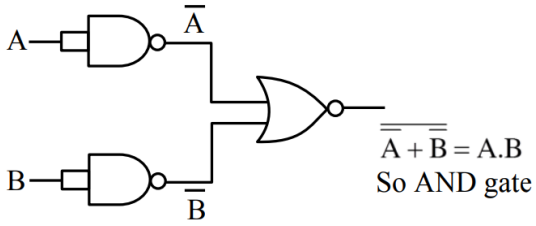
Ans 10.



$Y = A \cdot B + \bar{B}$

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

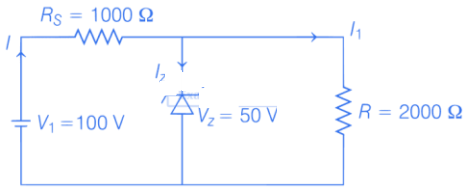
Ans 11.



Ans 12.

$$\text{Band gap} = \frac{hc}{\lambda} = 2 \text{ eV}$$

Ans 13. Consider the given figure and draw the direction of current as follows



Here, current I is flowing through resistance R_s and I_1 is the current flowing through R = 2000 Ω

$$\therefore \text{Current, } I = \frac{V_i - V_z}{R_s} \Rightarrow I = \frac{100-50}{1000}$$

= 50 mA .... (i)

[∵ Resistance and Zener diode are in parallel, therefore voltages across them are same]

and current, $I_1 = \frac{50}{2000} = 25$ mA .... (ii)

By using Kirchhoff's current law,

$\because I = I_1 + I_z$

$\Rightarrow I_z = I - I_1$ ..... (iii)

From Eq. (i) and (ii) and, we get

$\Rightarrow I_z = (50 - 25)$ mA

$I_z = 25$ mA

Ans 14.

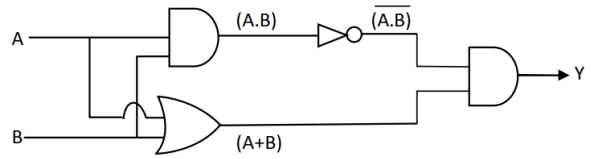
$$\alpha = \frac{I_C}{I_E} \& \beta = \frac{I_C}{I_B} \& I_E = I_B + I_C$$

$$\therefore \frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

$$\Rightarrow \frac{1}{\alpha} = \frac{1}{\beta} + 1 = \frac{1+\beta}{\beta}$$

$$\Rightarrow \alpha = \frac{\beta}{1+\beta}$$

Ans 15.



$$y = \left(\overline{A.B}\right) . (A + B)$$

$$= \left(\overline{A} + \overline{B}\right) . (A + B)$$

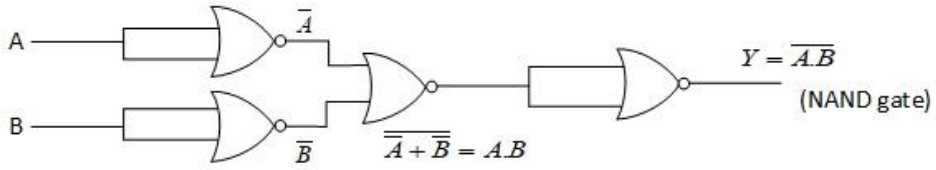
$$= \overline{A}A + \overline{A}B + A\overline{B} + \overline{B}B$$

$$= 0 + \overline{A}B + A\overline{B} + 0$$

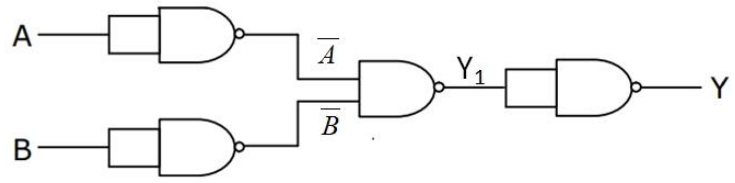
$$y = \overline{A}B + A\overline{B}$$

which is XOR gate

Ans 16.



Ans 17.



Output of first NAND gate with input A

$$= \overline{A.A}$$
$$= \overline{A} + \overline{A}$$
$$= \overline{A}$$

Similarly, Output of first NAND gate with input B

$$= \overline{B}$$

$$Y_1 = \overline{\overline{A}.\overline{B}}$$
$$= \overline{\overline{A}} + \overline{\overline{B}}$$
$$= A + B$$

$$Y = \overline{(A+B).(A+B)}$$
$$= \overline{(A+B)} + \overline{(A+B)}$$
$$= \overline{(A+B)}$$

So, given logic gates circuit is a NOR gate.

Ans 18.

$Y = \overline{\overline{A} + B} = A.\overline{B}$

A = 0 ⇒ Y = 0 for B = 0 or B = 1

A = 1 ⇒ Y = 0 for B = 1

A = 1 ⇒ Y = 1 for B = 0

Hence output is 1 only when input A = 1 and B = 0.

∴ A is the correct output.

Ans 19.

We know that $E = \frac{hc}{\lambda}$

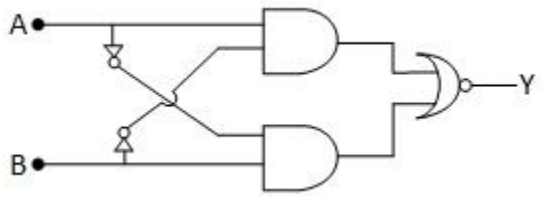
$$\lambda = \frac{hc}{E} \Rightarrow \frac{1240(in\ eV)}{E(in\ eV)}$$

$$\lambda = \frac{1240}{1.9}$$

= 652.63 nm ≈ 654 nm

Wavelength of red light is 620 nm to 750 nm

Ans 20.



If A = B = 0, then output y = 1

If A = B = 1, then output y = 1

Ans 21. In n-type semiconductor pentavalent impurity is added. Each pentavalent impurity donates a free electron. So the Fermi-level of n-type semiconductor will go upward.

And In p-type semiconductor trivalent impurity is added. Each trivalent impurity creates a hole in the valence band. So the Fermi-level of p-type semiconductor will go downward.

Ans 22. Since silicon diode is used so 0.7 Volt is drop across it, only D_1 will conduct.

So current through cell,

$$I = \frac{5-0.7}{10} = 0.43\ A$$

Ans 23. The zener breakdown occurs in the heavily doped p-n junction diode. Heavily doped p-n junction diodes have narrow depletion region.

Ans 24. S-1 :

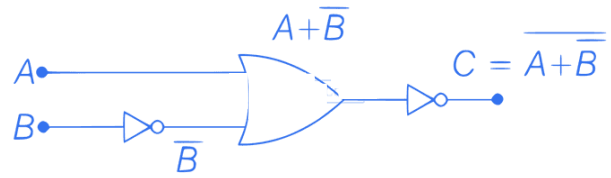
Statement 1 is false because in case of two discrete back to back connected diodes, there are four doped regions instead of three and there is nothing that resembles a thin base region between an emitter and a collector.

S-2 :

Statement-2 is true, as we know that, amplification factor (β) is the ratio of collector current to base current.

$$\beta = \frac{I_C}{I_B}$$

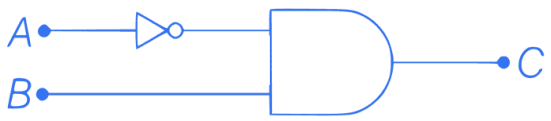
Ans 25. The logic circuit is given as



By using De-morgan's theorem,

$$C = \overline{A + \overline{B}} = \overline{A}.\overline{\overline{B}} = \overline{A}.B$$

This relation can be shown by the circuit drawn below



Ans 26. Given, emitter current, I_E = 4 mA

Collector current, I_C = 3.5 mA

Current gain in common base amplifier,

$$\alpha = \frac{I_C}{I_E}$$

$$\Rightarrow \alpha = \frac{3.5}{4} = \frac{7}{8}$$

Also, current gain in common emitter amplifier,

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\Rightarrow \beta = \frac{7/8}{1-7/8}$$

$$\beta = 7$$

TOPIC 1 Solids, Semiconductors and P-N Junction Diode

1. With increasing biasing voltage of a photodiode, the photocurrent magnitude : **[Sep. 05, 2020 (I)]**

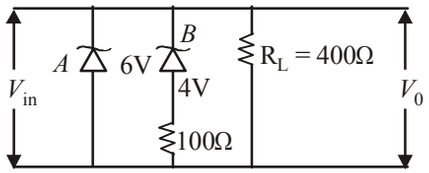
(a) remains constant

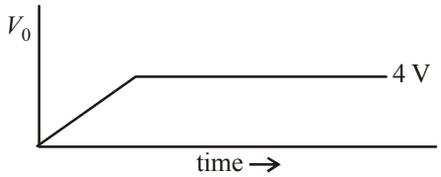
(b) increases initially and after attaining certain value, it decreases

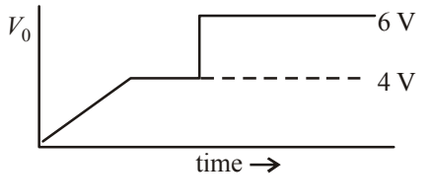
(c) Increases linearly

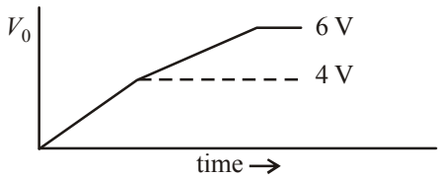
(d) increases initially and saturates finally

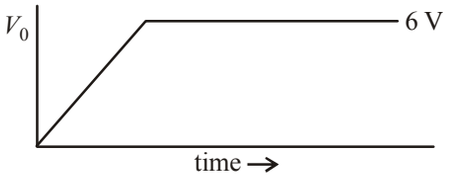
2. Two Zener diodes (A and B) having breakdown voltages of 6 V and 4 V respectively, are connected as shown in the circuit below. The output voltage V_0 variation with input voltage linearly increasing with time, is given by :
($V_{input} = 0$ V at $t = 0$)
(figures are qualitative) **[Sep. 05, 2020 (II)]**



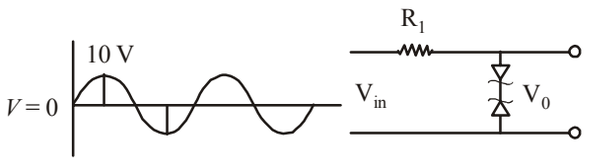
(a)


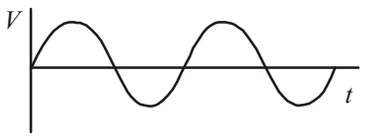
(b)


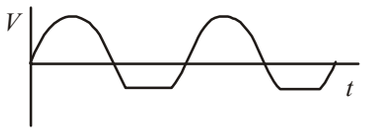
(c)


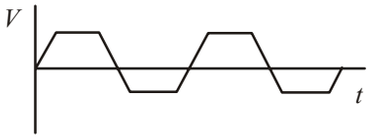
(d)


3. Take the breakdown voltage of the zener diode used in the given circuit as 6V. For the input voltage shown in figure below, the time variation of the output voltage is :
(Graphs drawn are schematic and not to scale)
[Sep. 04, 2020 (I)]



(a)


(b)


(c)


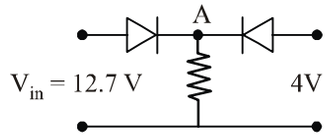
(d)


4. When a diode is forward biased, it has a voltage drop of 0.5 V. The safe limit of current through the diode is 10 mA. If a battery of emf 1.5 V is used in the circuit, the value of minimum resistance to be connected in series with the diode so that the current does not exceed the safe limit is : **[Sep. 03, 2020 (I)]**

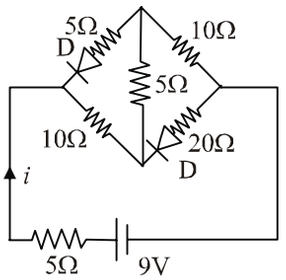
(a) 300 Ω (b) 50 Ω
(c) 100 Ω (d) 200 Ω

5. If a semiconductor photodiode can detect a photon with a maximum wavelength of 400 nm, then its band gap energy is:
Planck's constant, $h = 6.63 \times 10^{-34}$ J.s.
Speed of light, $c = 3 \times 10^8$ m/s **[Sep. 03, 2020 (II)]**
(a) 1.1 eV (b) 2.0 eV
(c) 1.5 eV (d) 3.1 eV

6. Both the diodes used in the circuit shown are assumed to be ideal and have negligible resistance when these are forward biased. Built in potential in each diode is 0.7 V. For the input voltages shown in the figure, the voltage (in Volts) at point A is _____. **[NA 9 Jan. 2020 I]**

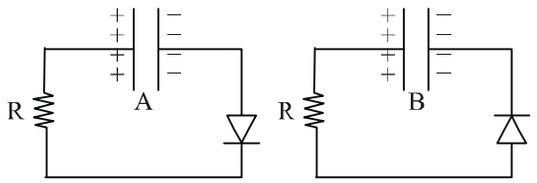


7. The current i in the network is: **[9 Jan. 2020 II]**



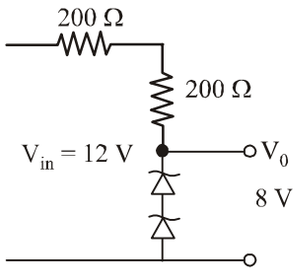
(a) 0.2 A (b) 0.6 A (c) 0.3 A (d) 0 A

8. Two identical capacitors A and B, charged to the same potential 5V are connected in two different circuits as shown below at time $t = 0$. If the charge on capacitors A and B at time $t = CR$ is Q_A and Q_B respectively, then (Here e is the base of natural logarithm) **[9 Jan. 2020 II]**

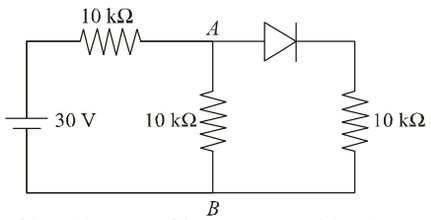


(a) $Q_A = \frac{VC}{e}, Q_B = \frac{CV}{2}$ (b) $Q_A = VC, Q_B = CV$
(c) $Q_A = VC, Q_B = \frac{VC}{e}$ (d) $Q_A = \frac{CV}{2}, Q_B = \frac{VC}{e}$

9. The circuit shown below is working as a 8 V dc regulated voltage source. When 12 V is used as input, the power dissipated (in mW) in each diode is; (considering both zener diodes are identical) _____. **[NA 9 Jan. 2020 II]**

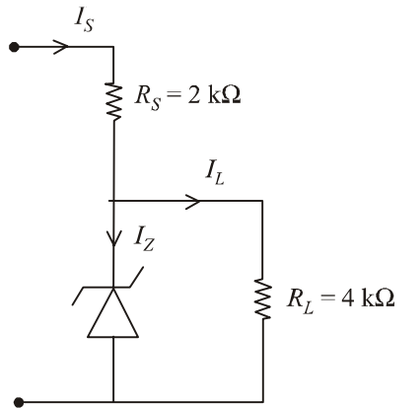


10. In the figure, potential difference between A and B is: **[7 Jan. 2020 II]**



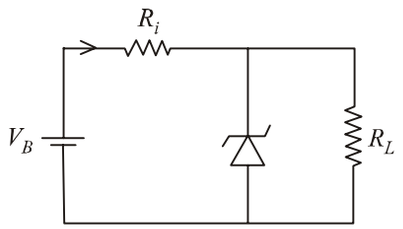
(a) 10 V (b) 5 V (c) 15 V (d) zero

11. Figure shows a DC voltage regulator circuit, with a Zener diode of breakdown voltage = 6V. If the unregulated input voltage varies between 10 V to 16 V, then what is the maximum Zener current ? **[12 Apr. 2019 II]**



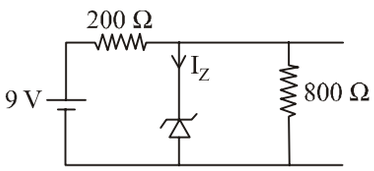
(a) 2.5 mA (b) 1.5 mA (c) 7.5 mA (d) 3.5 mA

12. The figure represents a voltage regulator circuit using a Zener diode. The breakdown voltage of the Zener diode is 6 V and the load resistance is $R_L = 4$ k. The series resistance of the circuit is R_i=1k. If the battery voltage V_B varies from 8 V to 16 V, what are the minimum and maximum values of the current through Zener diode ? **[10 Apr. 2019 II]**



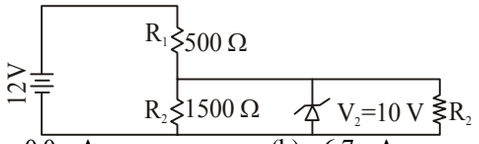
(a) 0.5 mA; 6 mA (b) 1 mA; 8.5 mA
(c) 0.5 mA; 8.5 mA (d) 1.5 mA; 8.5 mA

13. The reverse breakdown voltage of a Zener diode is 5.6 V in the given circuit.



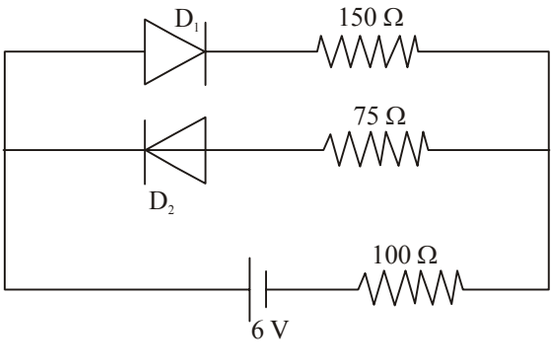
The current I_z through the Zener is : **[8 April 2019 I]**
(a) 10 mA (b) 17 mA
(c) 15 mA (d) 7 mA

14. In the given circuit the current through Zener Diode is close to : **[11 Jan. 2019 I]**



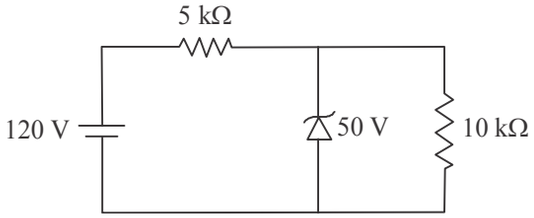
(a) 0.0 mA (b) 6.7 mA
(c) 4.0 mA (d) 6.0 mA

15. The circuit shown below contains two ideal diodes, each with a forward resistance of 50 Ω. If the battery voltage is 6V, the current through the 100 Ω resistance (in Amperes) is : **[11 Jan. 2019 II]**



(a) 0.036 (b) 0.020
(c) 0.027 (d) 0.030

16. For the circuit shown below, the current through the Zener diode is: **[10 Jan. 2019 II]**

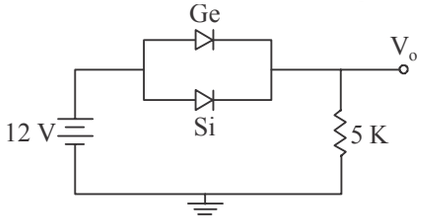


(a) 9 mA (b) 5 mA
(c) Zero (d) 14 mA

17. Mobility of electrons in a semiconductor is defined as the ratio of their drift velocity to the applied electric field. If, for an n-type semiconductor, the density of electrons is 10^{19} m^{-3} and their mobility is $1.6 m^2/(V.s)$ then the resistivity of the semiconductor (since it is an n-type semiconductor contribution of holes is ignored) is close to: **[9 Jan. 2019 I]**

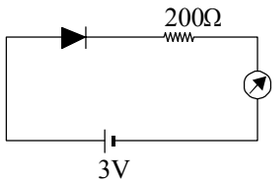
(a) 2 Ωm (b) 4 Ωm (c) 0.4 Ωm (d) 0.2 Ωm

18. Ge and Si diodes start conducting at 0.3 V and 0.7 V respectively. In the following figure if Ge diode connection are reversed, the value of V_o changes by : (assume that the Ge diode has large breakdown voltage) **[9 Jan. 2019 II]**



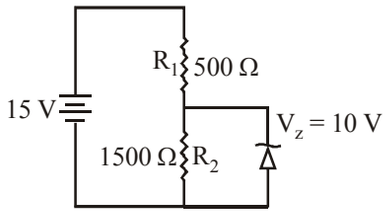
(a) 0.8 V (b) 0.6 V
(c) 0.2 V (d) 0.4 V

19. The reading of the ammeter for a silicon diode in the given circuit is : **[2018]**



(a) 0 (b) 15 mA
(c) 11.5 mA (d) 13.5 mA

20. In the given circuit, the current through zener diode is: **[Online April 16, 2018]**



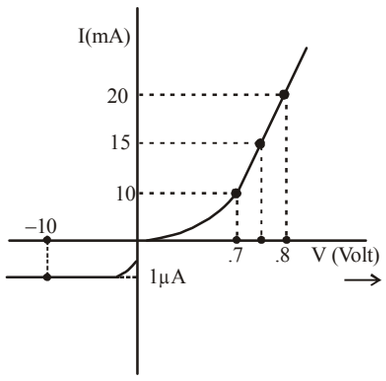
(a) 2.5mA (b) 3.3mA
(c) 5.5mA (d) 6.7mA

21. What is the conductivity of a semiconductor sample having electron concentration of 5×10^{18} m^{-3}, hole concentration of 5×10^{19} m^{-3}, electron mobility of 2.0 $m^2 V^{-1} s^{-1}$ and hole mobility of 0.01 $m^2 V^{-1} s^{-1}$? **[Online April 8, 2017]**

(Take charge of electron as 1.6×10^{-19} C)

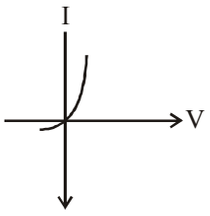
(a) $1.68\ (\Omega - m)^{-1}$ (b) $1.83\ (\Omega - m)^{-1}$
(c) $0.59\ (\Omega - m)^{-1}$ (d) $1.20\ (\Omega - m)^{-1}$

22. The V–I characteristic of a diode is shown in the figure. The ratio of forward to reverse bias resistance is : **[Online April 8, 2017]**

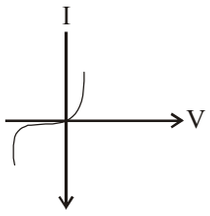


(a) 10 (b) 10^{-6}
(c) 10^6 (d) 100

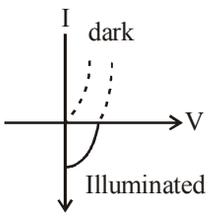
23. Identify the semiconductor devices whose characteristics are given below, in the order (i), (ii), (iii), (iv) : **[2016]**



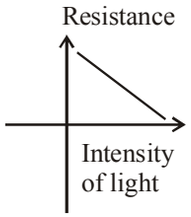
(i)



(ii)



(iii)



(iv)

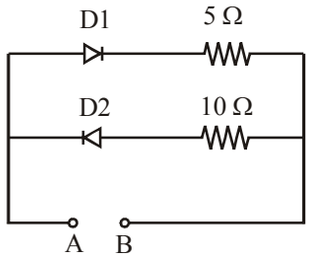
(a) Solar cell, Light dependent resistance, Zener diode, simple diode
(b) Zener diode, Solar cell, simple diode, Light dependent resistance
(c) Simple diode, Zener diode, Solar cell, Light dependent resistance
(d) Zener diode, Simple diode, Light dependent resistance, Solar cell

24. The temperature dependence of resistances of Cu and undoped Si in the temperature range 300-400 K, is best described by : **[2016]**
(a) Linear increase for Cu, exponential decrease of Si.
(b) Linear decrease for Cu, linear decrease for Si.
(c) Linear increase for Cu, linear increase for Si.
(d) Linear increase for Cu, exponential increase for Si.

25. An experiment is performed to determine the I–V characteristics of a Zener diode, which has a protective resistance of R = 100 Ω, and a maximum power of dissipation rating of 1W. The minimum voltage range of the DC source in the circuit is : **[Online April 9, 2016]**
(a) 0–5V (b) 0–24 V
(c) 0–12 V (d) 0–8V

26. A red LED emits light at 0.1 watt uniformly around it. The amplitude of the electric field of the light at a distance of 1 m from the diode is : **[2015]**
(a) 5.48 V/m (b) 7.75 V/m
(c) 1.73 V/m (d) 2.45 V/m

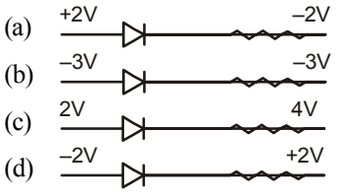
27. A 2V battery is connected across AB as shown in the figure. The value of the current supplied by the battery when in one case battery's positive terminal is connected to A and in other case when positive terminal of battery is connected to B will respectively be:
[Online April 11, 2015]



(a) 0.4 A and 0.2 A (b) 0.2 A and 0.4 A
(c) 0.1 A and 0.2 A (d) 0.2 A and 0.1 A

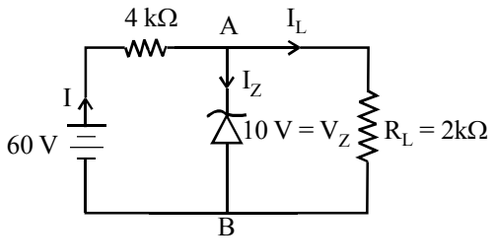
28. In an unbiased n-p junction electrons diffuse from n-region to p-region because : **[Online April 10, 2015]**
(a) holes in p-region attract them
(b) electrons travel across the junction due to potential difference
(c) only electrons move from n to p region and not the vice-versa
(d) electron concentration in n-region is more compared to that in p-region

29. The forward biased diode connection is: **[2014]**



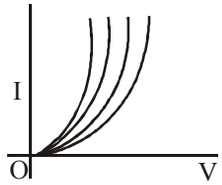
30. For LED's to emit light in visible region of electromagnetic light, it should have energy band gap in the range of:
[Online April 12, 2014]
(a) 0.1 eV to 0.4 eV (b) 0.5 eV to 0.8 eV
(c) 0.9 eV to 1.6 eV (d) 1.7 eV to 3.0 eV

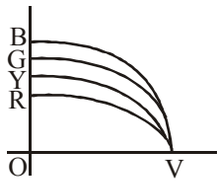
31. A Zener diode is connected to a battery and a load as show below: **[Online April 11, 2014]**



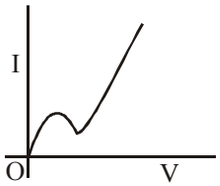
The currents, I, I_Z and I_L are respectively.
(a) 15 mA, 5 mA, 10 mA
(b) 15 mA, 7.5 mA, 7.5 mA
(c) 12.5 mA, 5 mA, 7.5 mA
(d) 12.5 mA, 7.5 mA, 5 mA

32. The I-V characteristic of an LED is **[2013]**

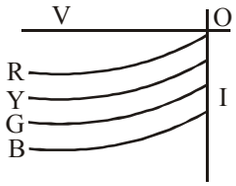
(a)


(b)


(c)

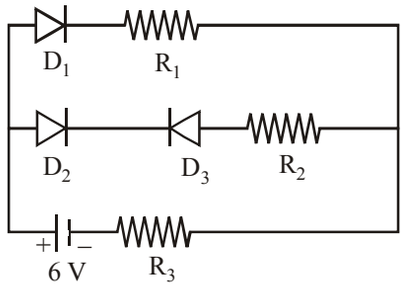


(d)



33. Figure shows a circuit in which three identical diodes are used. Each diode has forward resistance of 20 Ω and infinite backward resistance. Resistors $R_1 = R_2 = R_3 = 50\,\Omega$. Battery voltage is 6 V. The current through R_3 is :

[Online April 22, 2013]



(a) 50 mA (b) 100 mA
(c) 60 mA (d) 25 mA

34. This question has Statement 1 and Statement 2. Of the four choices given after the Statements, choose the one that best describes the two Statements.

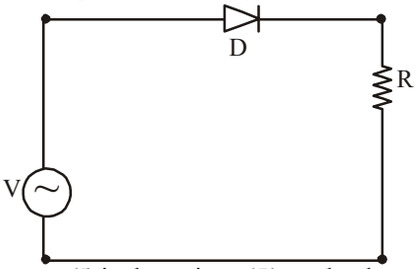
Statement 1: A pure semiconductor has negative temperature coefficient of resistance.

Statement 2: On raising the temperature, more charge carriers are released into the conduction band.

[Online May 12, 2012]

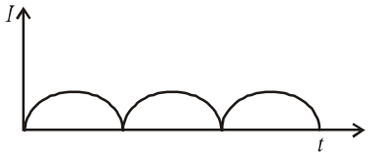
(a) Statement 1 is false, Statement 2 is true.
(b) Statement 1 is true, Statement 2 is false.
(c) Statement 1 is true, Statement 2 is true, Statement 2 is not a correct explanation of Statement 1.
(d) Statement 1 is true, Statement 2 is true, Statement 2 is the correct explanation of Statement 1.

35. A *p-n* junction (*D*) shown in the figure can act as a rectifier. An alternating current source (*V*) is connected in the circuit.

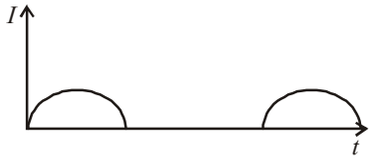


The current (*I*) in the resistor (*R*) can be shown by : **[2009]**

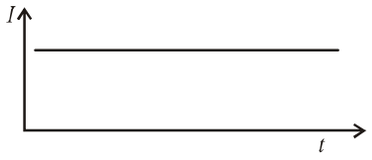
(a)



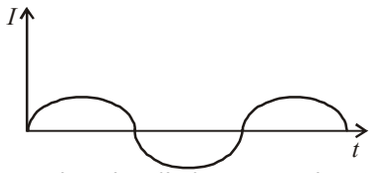
(b)



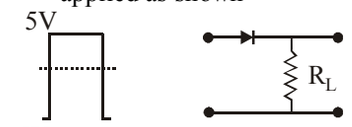
(c)



(d)

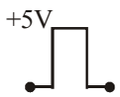


36. If in a *p-n* junction diode, a square input signal of 10 V is applied as shown **[2007]**

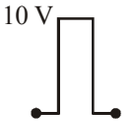


Then the output signal across R_L will be

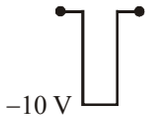
(a)



(b)



(c)

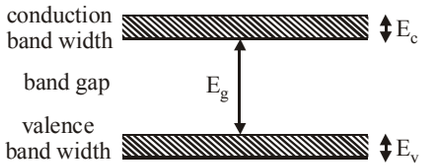


(d)

37. Carbon, silicon and germanium have four valence electrons each. At room temperature which one of the following statements is most appropriate ? **[2007]**

(a) The number of free electrons for conduction is significant only in Si and Ge but small in C.
(b) The number of free conduction electrons is significant in C but small in Si and Ge.
(c) The number of free conduction electrons is negligibly small in all the three.
(d) The number of free electrons for conduction is significant in all the three.

38. If the lattice constant of this semiconductor is decreased, then which of the following is correct? **[2006]**



(a) All E_c, E_g, E_v increase
(b) E_c and E_v increase, but E_g decreases
(c) E_c and E_v decrease, but E_g increases
(d) All E_c, E_g, E_v decrease

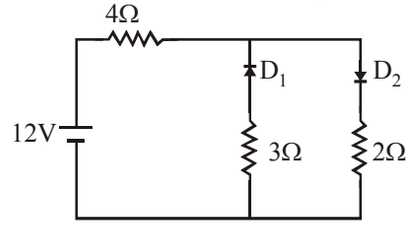
39. A solid which is not transparent to visible light and whose conductivity increases with temperature is formed by **[2006]**

(a) Ionic bonding
(b) Covalent bonding
(c) Vander Waals bonding
(d) Metallic bonding

40. If the ratio of the concentration of electrons to that of holes in a semiconductor is $\frac{7}{5}$ and the ratio of currents is $\frac{7}{4}$, then what is the ratio of their drift velocities? **[2006]**

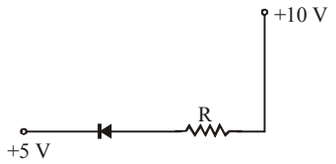
(a) $\frac{5}{8}$ (b) $\frac{4}{5}$ (c) $\frac{5}{4}$ (d) $\frac{4}{7}$

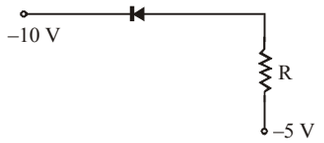
41. The circuit has two oppositively connected ideal diodes in parallel. What is the current flowing in the circuit? **[2006]**

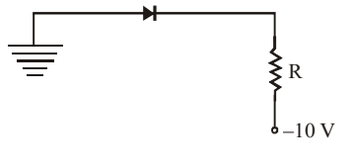


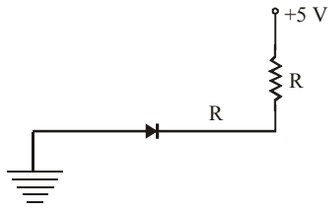
(a) 1.71A (b) 2.00A (c) 2.31A (d) 1.33A

42. In the following, which one of the diodes reverse biased? **[2006]**

(a)


(b)


(c)


(d)


43. The electrical conductivity of a semiconductor increases when electromagnetic radiation of wavelength shorter than 2480 nm is incident on it. The band gap in (eV) for the semiconductor is **[2005]**

(a) 2.5 eV (b) 1.1 eV (c) 0.7 eV (d) 0.5 eV

44. When p-n junction diode is forward biased then **[2004]**

(a) both the depletion region and barrier height are reduced
(b) the depletion region is widened and barrier height is reduced
(c) the depletion region is reduced and barrier height is increased
(d) Both the depletion region and barrier height are increased

45. A strip of copper and another of germanium are cooled from room temperature to 80K. The resistance of **[2003]**

(a) each of these decreases
(b) copper strip increases and that of germanium decreases
(c) copper strip decreases and that of germanium increases
(d) each of these increases

46. The difference in the variation of resistance with temeperature in a metal and a semiconductor arises essentially due to the difference in the **[2003]**

(a) crystal sturcture
(b) variation of the number of charge carriers with temperature
(c) type of bonding
(d) variation of scattering mechanism with temperature

47. In the middle of the depletion layer of a reverse- biased *p-n* junction, the **[2003]**

(a) electric field is zero
(b) potential is maximum
(c) electric field is maximum
(d) potential is zero

48. At absolute zero, Si acts as **[2002]**

(a) non-metal (b) metal
(c) insulator (d) none of these

49. By increasing the temperature, the specific resistance of a conductor and a semiconductor **[2002]**

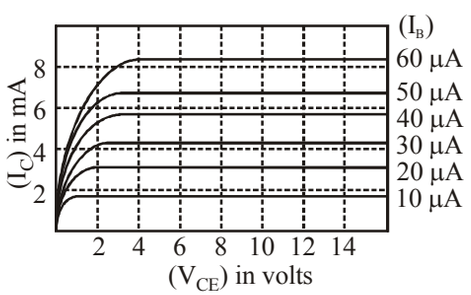
(a) increases for both (b) decreases for both
(c) increases, decreases (d) decreases, increases

50. The energy band gap is maximum in **[2002]**

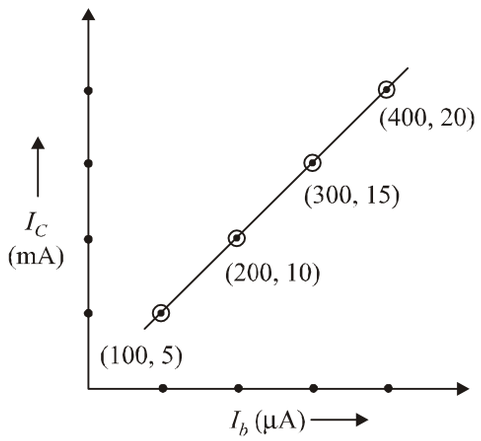
(a) metals (b) superconductors
(c) insulators (d) semiconductors.

TOPIC 2 Junction Transistor

51. The output characteristics of a transistor is shown in the figure. When V_{CE} is 10 V and $I_C = 4.0$ mA, then value of β_{ac} is _____. **[NA Sep. 06, 2020 (II)]**



52. The transfer characteristic curve of a transistor, having input and output resistance 100 Ω and 100 k Ω respectively, is shown in the figure. The Voltage and Power gain, are respectively : **[12 Apr. 2019 I]**



(a) $2.5\times10^4, 2.5\times10^6$ (b) $5\times10^4, 5\times10^6$
(c) $5\times10^4, 5\times10^5$ (d) $5\times10^4, 2.5\times10^6$

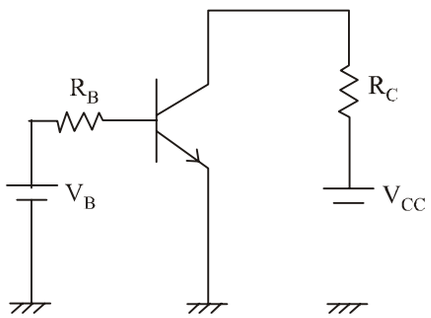
53. An npn transistor operates as a common emitter amplifier, with a power gain of 60 dB. The input circuit resistance is 100Ω and the output load resistance is 10 kΩ. The common emitter current gain β is : **[10 Apr. 2019 I]**

(a) 10^2 (b) 60 (c) 6×10^2 (d) 10^4

54. An NPN transistor is used in common emitterconfiguration as an amplifier with 1 k &! load resistance. Signal voltage of 10 mV is applied across the base-emitter. This produces a 3 mA change in the collector current and 15 ¼A change in the base current of the amplifier. The input resistance and voltage gain are: **[9 April 2019 I]**

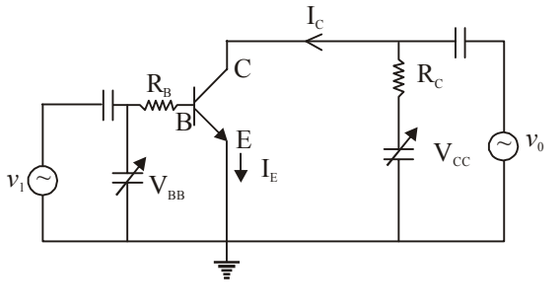
(a) 0.33 k Ω 1.5 (b) 0.67 k Ω 300
(c) 0.67 k Ω 200 (d) 0.33 k Ω 300

55. A common emitter amplifier circuit, built using an npn transistor, is shown in the figure. Its dc current gain is 250, $R_C = 1$ k &! and $V_{CC} = 10$V. What is the minimum base current for V_{CE} to reach saturation ? **[8 Apr. 2019 II]**



(a) 40 μA (b) 100 μA
(c) 7 μA (d) 10 μA

56.



In the figure, given that V_{BB} supply can vary from 0 to 5.0 V, V_{CC} = 5 V, $\beta_{dc} = 200$, $R_B = 100$ kΩ, $R_C = 1$ KΩ and $V_{BE} = 1.0$ V. The minimum base current and the input voltage at which the transistor will go to saturation, will be, respectively : **[12 Jan. 2019 II]**

(a) 25 μA and 3.5 V (b) 20 μA and 3.5 V
(c) 25 μA and 2.8 V (d) 20 μA and 2.8 V

57. In a common emitter configuration with suitable bias, it is given than R_L is the load resistance and R_{BE} is small signal dynamic resistance (input side). Then, voltage gain, current gain and power gain are given, respectively, by:
(β is current gain, I_B, I_C, I_E are respectively base, collector and emitter currents:) **[Online April 15, 2018]**

(a) $\beta\frac{R_L}{R_{BE}}, \frac{\Delta I_E}{\Delta I_B}, \beta^2\frac{R_L}{R_{BE}}$

(b) $\beta^2\frac{R_L}{R_{BE}}, \frac{\Delta I_C}{\Delta I_B}, \beta\frac{R_L}{R_{BE}}$

(c) $\beta^2\frac{R_L}{R_{BE}}, \frac{\Delta I_C}{\Delta I_E}, \beta^2\frac{R_L}{R_{BE}}$

(d) $\beta\frac{R_L}{R_{BE}}, \frac{\Delta I_C}{\Delta I_B}, \beta^2\frac{R_L}{R_{BE}}$

58. The current gain of a common emitter amplifier is 69. If the emitter current is 7.0 mA, collector current is : **[Online April 9, 2017]**

(a) 9.6 mA (b) 6.9 mA
(c) 0.69 mA (d) 69 mA

59. In a common emitter amplifier circuit using an n-p-n transistor, the phase difference between the input and the output voltages will be : **[Online April 2, 2017]**

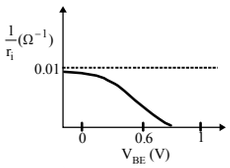
(a) 135° (b) 180°
(c) 45° (d) 90°

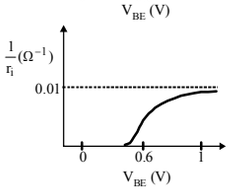
60. For a common emitter configuration, if α and β have their usual meanings, the incorrect relationship between α and β is : **[2016]**

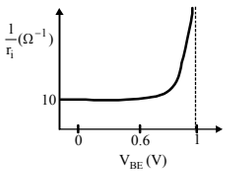
(a) $a = \frac{b}{1+b}$ (b) $a = \frac{b^2}{1+b^2}$

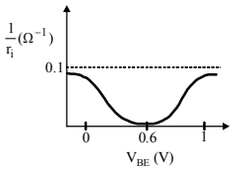
(c) $\frac{1}{a} = \frac{1}{b} + 1$ (d) None of these

61. A realistic graph depicting the variation of the reciprocal of input resistance in an input characteristics measurement in a common emitter transistor configuration is : **[Online April 10, 2016]**

(a) 

(b) 

(c) 

(d) 

62. The ratio (R) of output resistance r_0, and the input resistance r_i in measurements of input and output characteristics of a transistor is typically in the range : **[Online April 10, 2016]**

(a) $R \sim 10^2 - 10^3$ (b) $R \sim 1 - 10$
(c) $R \sim 0.1 - 1.0$ (d) $R \sim 0.1 - 0.01$

63. An unknown transistor needs to be identified as a npn or pnp type. A multimeter, with +ve and –ve terminals, is used to measure resistance between different terminals of transistor. If terminal 2 is the base of the transistor then which of the following is correct for a pnp transistor? **[Online April 9, 2016]**

(a) +ve terminal 2, –ve terminal 3,resistance low
(b) +ve terminal 2, –ve terminal 1, resistane high
(c) +ve terminal 1, –ve terminal 2, resistance high
(d) +ve terminal 3, –ve terminal 2, resistance high

64. An n-p-n transistor has three leads A, B and C. Connecting B and C by moist fingers, A to the positive lead of an ammeter, and C to the negative lead of the ammeter, one finds large deflection. Then, A, B and C refer respectively to: **[Online April 9, 2014]**

(a) Emitter, base and collector
(b) Base, emitter and collector
(c) Base, collector and emitter
(d) Collector, emitter and base.

65. A working transistor with its three legs marked *P*, *Q* and *R* is tested using a multimeter. No conduction is found between *P* and *Q*. By connecting the common (negative) terminal of the multimeter to *R* and the other (positive) terminal to *P* or *Q*, some resistance is seen on the multimeter. Which of the following is true for the transistor? **[2008]**

(a) It is an npn transistor with *R* as base
(b) It is a pnp transistor with *R* as base
(c) It is a pnp transistor with *R* as emitter
(d) It is an npn transistor with *R* as collector

66. In a common base mode of a transistor, the collector current is 5.488 mA for an emitter current of 5.60 mA. The value of the base current amplification factor (β) will be **[2006]**

(a) 49 (b) 50
(c) 51 (d) 48

67. In a common base amplifier, the phase difference between the input signal voltage and output voltage is **[2005]**

(a) π (b) $\frac{\pi}{4}$
(c) $\frac{\pi}{2}$ (d) 0

68. When npn transistor is used as an amplifier **[2004]**

(a) electrons move from collector to base
(b) holes move from emitter to base
(c) electrons move from base to collector
(d) holes move from base to emitter

69. For a transistor amplifier in common emitter configuration for load impedance of 1k Ω $(h_{fe} = 50$ and $h_{oe} = 25)$ the current gain is **[2004]**

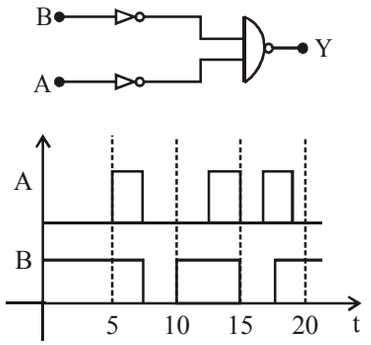
(a) –24.8 (b) –15.7
(c) –5.2 (d) –48.78

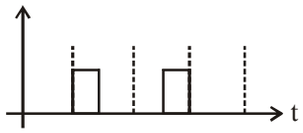
70. The part of a transistor which is most heavily doped to produce large number of majority carriers is **[2002]**

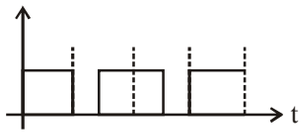
(a) emmiter
(b) base
(c) collector
(d) can be any of the above three.

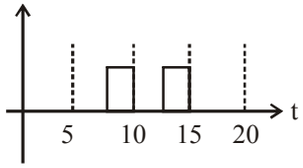
TOPIC 3 Digital Electronics and Logic Gates

71. Identify the correct output signal Y in the given combination of gates (as shown) for the given inputs A and B. **[Sep. 06, 2020 (I)]**



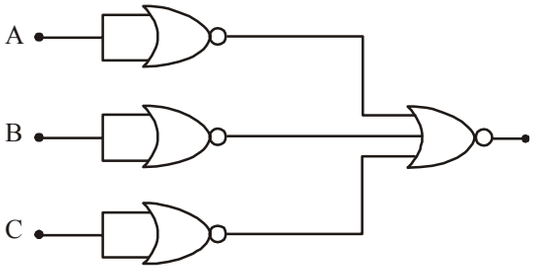
(a)


(b)


(c)


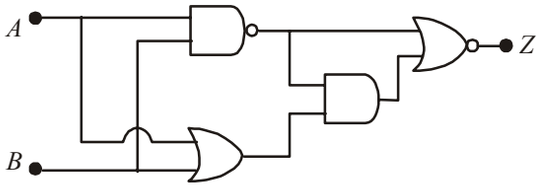
(d)


72. Identify the operation performed by the circuit given below:
[Sep. 04, 2020 (II)]



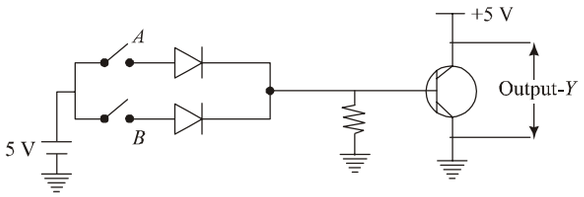
(a) NAND (b) OR
(c) AND (d) NOT

73. In the following digitial circuit, what will be the output at 'Z', when the input (A, B) are (1, 0), (0, 0), (1, 1), (0, 1) :
[Sep. 02, 2020 (II)]



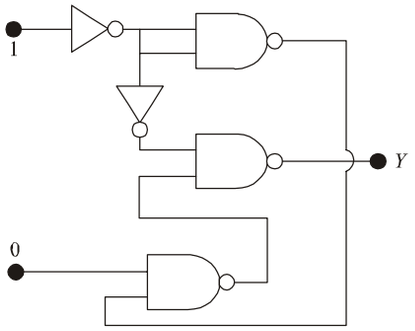
(a) 0, 0, 1, 0 (b) 1, 0, 1, 1
(c) 1, 1, 0, 1 (d) 0, 1, 0, 0

74. Boolean relation at the output stage-Y for the following circuit is: **[8 Jan. 2020 I]**



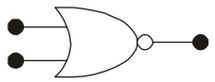
(a) $\overline{A}+\overline{B}$ (b) $A+B$
(c) $A.B$ (d) $\overline{A}.\overline{B}$

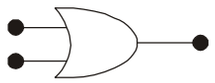
75. In the given circuit, value of Y is: **[8 Jan. 2020 II]**

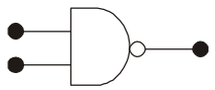


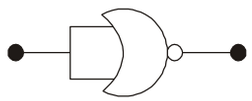
(a) 0
(b) toggles between 0 and 1
(c) will not execute
(d) 1

76. Which of the following gives a reversible operation?
[7 Jan. 2020 I]

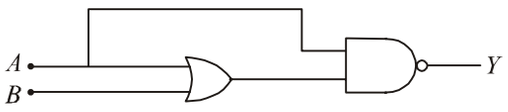
(a)


(b)


(c)


(d)


77. The truth table for the circuit given in the fig. is :
[9 April 2019 I]



(a)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	1

(b)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

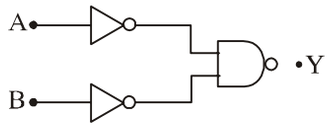
(c)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

(d)

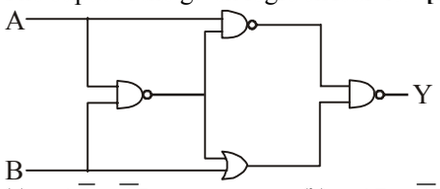
A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

78. The logic gate equivalent to the given logic circuit is:
[9 Apr. 2019 II]



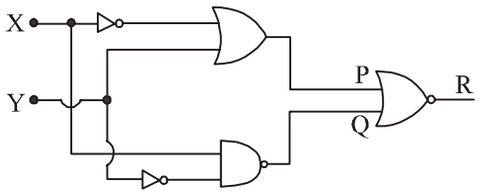
(a) NAND (b) OR (c) NOR (d) AND

79. The ouput of the given logic cirfcuit is: **[12 Jan. 2019 I]**



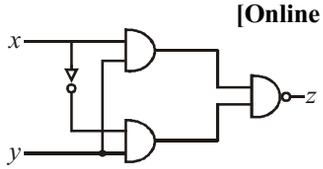
(a) $A\bar{B} + \bar{A}B$ (b) $AB + \bar{A}B$
(c) $A\bar{B}$ (d) $\bar{A}B$

80. To get output '1' at R, for the given logic gate circuit the input values must be: **[10 Jan. 2019 I]**



(a) X = 0, Y = 1 (b) X = 1, Y = 1
(c) X = 1, Y = 0 (d) X = 0, Y = 0

81. Truth table for the given circuit will be
[Online April 15, 2018]



(a)

x	y	z
0	0	1
0	1	1
1	0	1
1	1	0

(b)

x	y	z
0	0	0
0	1	0
1	0	0
1	1	1

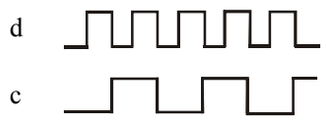
(c)

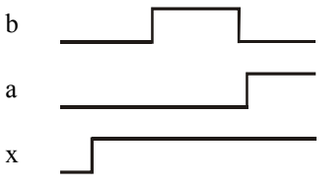
x	y	z
0	0	1
0	1	1
1	0	1
1	1	1

(d)

x	y	z
0	0	0
0	1	1
1	0	1
1	1	1

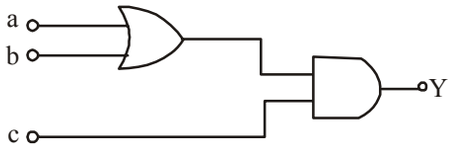
82. If a, b, c, d are inputs to a gate and x is its output, then, as per the following time graph, the gate is : **[2016]**





(a) OR (b) NAND
(c) NOT (d) AND

83. To get an output of 1 from the circuit shown in figure the input must be : **[Online April 10, 2016]**



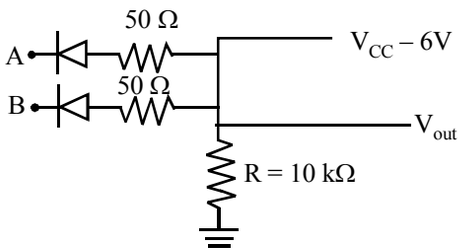
(a) a = 0, b = 0, c = 1 (b) a = 1, b = 0, c = 0
(c) a = 1, b = 0, c = 1 (d) a = 0, b = 1, c = 0

84. The truth table given in fig. represents :
[Online April 9, 2016]

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(a) OR – Gate (b) NAND– Gate
(c) AND– Gate (d) NOR– Gate

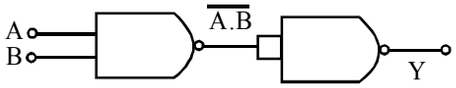
85.



Given: A and B are input terminals.
Logic 1 = > 5 V
Logic 0 = < 1 V
Which logic gate operation, the above circuit does?
[Online April 19, 2014]

(a) AND Gate (b) OR Gate
(c) XOR Gate (d) NOR Gate

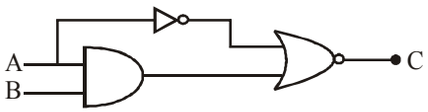
86. Identify the gate and match A, B, Y in bracket to check.
[Online April 9, 2014]

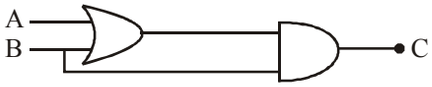


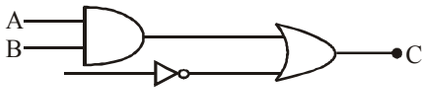
(a) AND (A = 1, B = 1, Y = 1)
(b) OR (A = 1, B = 1, Y = 0)
(c) NOT (A = 1, B = 1, Y = 1)
(d) XOR (A = 0, B = 0, Y = 0)

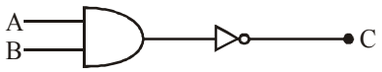
87. Which of the following circuits correctly represents the following truth table ? **[Online April 25, 2013]**

A	*B*	*C*
0	0	0
0	1	0
1	0	1
1	1	0

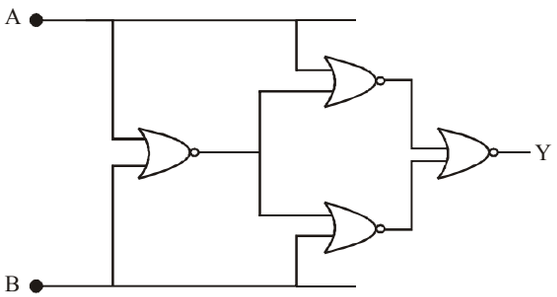
(a) 

(b) 

(c) 

(d) 

88. A system of four gates is set up as shown. The 'truth table' corresponding to this system is : **[Online April 23, 2013]**



(a)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(b)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	0

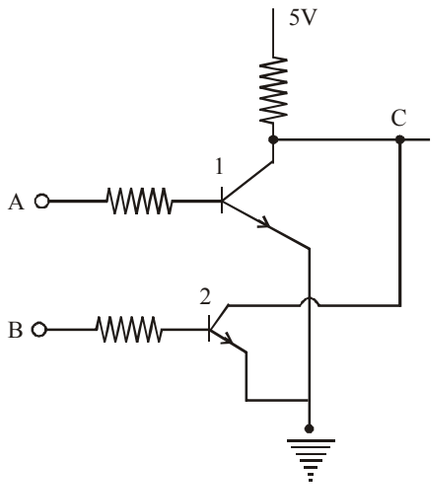
(c)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

(d)

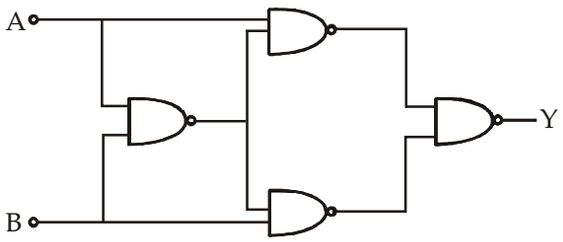
A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

89. Consider two *npn* transistors as shown in figure. If 0 Volts corresponds to false and 5 Volts correspond to true then the output at C corresponds to : **[Online April 9, 2013]**



(a) A NAND B (b) A OR B
(c) A AND B (d) A NOR B

90. Truth table for system of four NAND gates as shown in figure is : **[2012]**



(a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(b)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

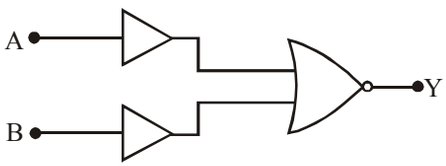
(c)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

(d)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

91. The figure shows a combination of two NOT gates and a NOR gate. **[Online May 26, 2012]**



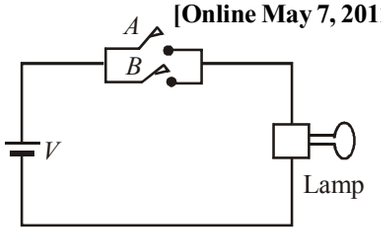
The combination is equivalent to a
(a) NAND gate (b) NOR gate
(c) AND gate (d) OR gate

92. Which one of the following is the Boolean expression for NOR gate? **[Online May 19, 2012]**

(a) $Y = \overline{A + B}$ (b) $Y = \overline{A.B}$

(c) $Y = A.B$ (d) $Y = \overline{A}$

93. Which logic gate with inputs A and B performs the same operation as that performed by the following circuit? **[Online May 7, 2012]**



(a) NAND gate

(b) OR gate

(c) NOR gate

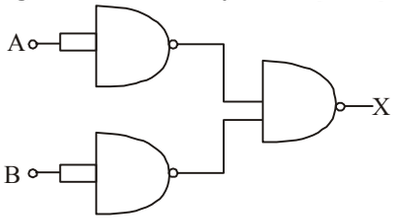
(d) AND gate

94. The output of an OR gate is connected to both the inputs of a NAND gate. The combination will serve as a: **[2011 RS]**

(a) NOT gate (b) NOR gate

(c) AND gate (d) OR gate

95. The combination of gates shown below yields **[2010]**



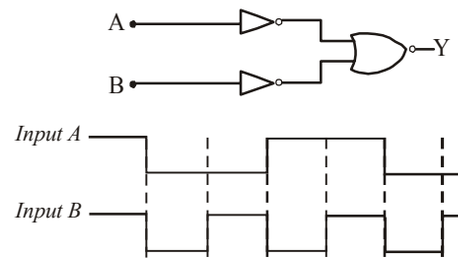
(a) OR gate

(b) NOT gate

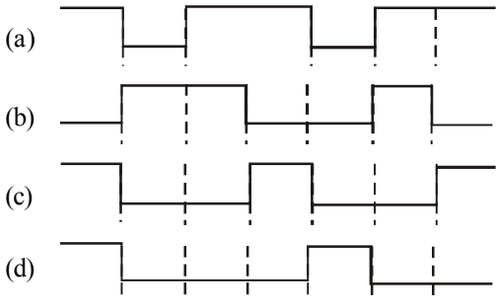
(c) XOR gate

(d) NAND gate

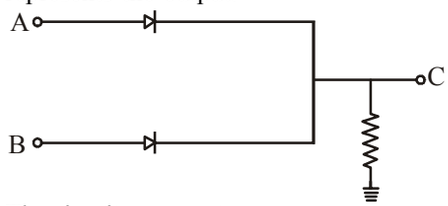
96. The logic circuit shown below has the input waveforms 'A' and 'B' as shown. Pick out the correct output waveform. **[2009]**



Output is



97. In the circuit below, A and B represent two inputs and C represents the output. **[2008]**



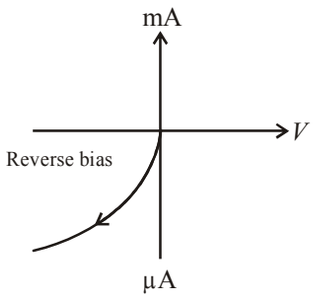
The circuit represents

(a) NOR gate (b) AND gate

(c) NAND gate (d) OR gate

Hints & Solutions

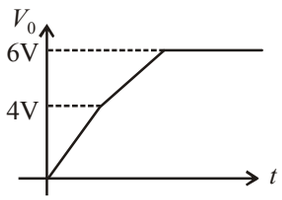
1. **(d)** I-V characteristic of a photodiode is as follows :



On increasing the biasing voltage of a photodiode, the magnitude of photocurrent first increases and then attains a saturation.

2. **(c)** Till input voltage reaches 4 V. No zener is in breakdown region so $V_0 = V_i$. Then now when V_i changes between 4 V to 6 V one zener with 4 V will breakdown and P.D. across this zener will become constant and remaining potential will dorp across resistance in series with 4 V zener.

Now current in circuit increases abruptly and source must have an internal resistance due to which some potential will get drop across the source also so correct graph between V_0 and t will be



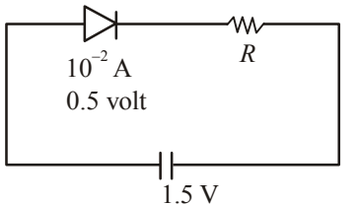
3. **(c)** Here two zener diodes are in reverse polarity so if one is in forward bias the other will be in reverse bias and above 6V the reverse bias will too be in conduction mode. Hence when V > 6V the output will be constant. And when V < 6V it will follow the inut voltage.

4. **(c)** According to question, when diode is forward biased,

$V_{diode} = 0.5$ V

Safe limit of current, $I = 10$ mA $= 10^{-2}$ A

$R_{min} = ?$



Voltage through resistance

$V_R = 1.5 - 0.5 = 1$ volt

$iR = 1 (= V_R)$

$\therefore R_{min} = \frac{1}{i} = \frac{1}{10^{-2}} = 100\ \Omega$

5. **(d)** Given,

Wavelength of photon, $\lambda = 400$ nm

A photodiode can detect a wavelength corresponding to the energy of band gap. If the signal is having wavelength greater than this value, photodiode cannot detect it.

$\therefore$ Band gap $E_g = \frac{hc}{\lambda} = \frac{1237.5}{400} = 3.09$ eV

6. **(12)** Right hand diode is reversed biased and left hand diode is forward biased.

Hence Voltage at 'A'

$V_A = 12.7 - 0.7 = 12$ volt

7. **(c)** Both the diodes are reverse biased, so, there is no flow of current through 5Ω and 20Ω resistances.

Now, two resistors of 10Ω and two resistors of 5Ω are in series.

Hence current I through the network = 0.3 A

8. **(c)** In case I diode is reverse biased, so no current flows

$\therefore \quad Q_A = CV$

In case II, current will flow as diode is forward biased. So, it offers negligible resistance to the flow of current and thus be replaced by short circuit. Now, the charge of capacitor will leak through the resistance and decay exponentially with time.

During discharging of capacitor

Potential difference across the capacitor at any instant

$V' = Ve^{-\frac{t}{CR}}$

But $t = CR$

$V' = Ve^{-1} = \frac{V}{e}$

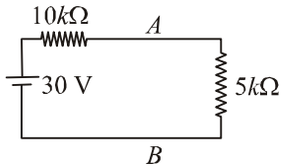
$\therefore \quad$ Charge $Q_B = CV' = \frac{CV}{e}$

9. **(40)** Current in the circuit, $I = \frac{12-8}{400} = 10^{-2}\ A$

Power dissipited in each diode, $P = VI$

$\Rightarrow \quad P = 4 \times 10^{-2} = 40\ mW$

10. **(a)** The given circuit has two $10k\Omega$ resistances in parallel, so we can reduce this parallel combination to a single equivalent resistance of $5k\Omega$.



Diode is in forward bias. So it will behave like a conducting wire.

$$V_A - V_B = \frac{30}{5+10} \times 5 = 10\,V$$

11. **(d)** Current in load resistance,

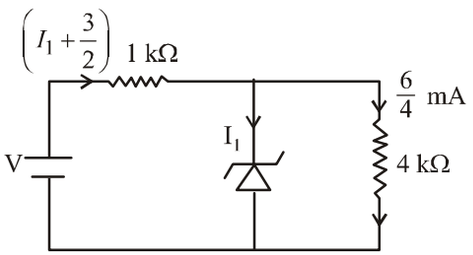
$$i_1 = \frac{6}{4\times10^3} = 1.5 \times 10^{-3}\,A = 1.5\,mA$$

For $V = 16$ volt,

$$i_s = \frac{(16-6)}{2\times10^3} = 5\,mA$$

$$\therefore \quad i_2 = i_s - i_1 = 5 - 1.5 = 3.5\,mA$$

12. **(c)**



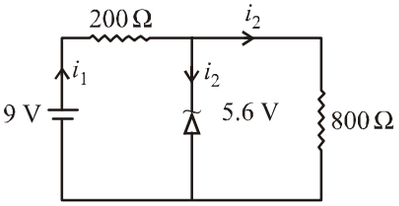
For voltage, V = 8V

$$\text{Current, } I_1 = \left(8-6-\frac{3}{2}\right) = \frac{1}{2} = 0.5\,mA$$

For voltage, V = 16V

$$\text{Current, } I_2 = \left(16-6-\frac{3}{2}\right) = 8.5\,mA$$

13. **(a)**



P.D. across 800Ω resistors = 5.6 V

$$\text{so, } I_{800\Omega} = \frac{5.6}{800} A = 7\,mA$$

Now, P.D. across 200Ω resistors = 9 – 5.6 V = 3.4 V

$$\text{so, } I_{200\Omega} = \frac{9-5.6}{200} = 17\,mA$$

so, current through zener diode = I_2 = 17 – 7 = 10 mA

14. **(a)** Since voltage across zener diode does not reach to breakdown voltage therefore its resistance will be infinite & current through it is 0.

15. **(b)** As D_2 is reversed biased, so no current through 75Ω resistor.

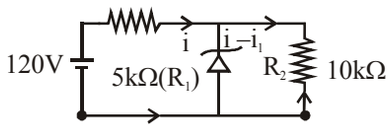
now $R_{eq} = 150 + 50 + 100$

$= 300\,\Omega$

$$\text{So, required current } I = \frac{\text{BatteryVoltage}}{300}$$

$$I = \frac{6}{300} = 0.02$$

16. **(a)** The voltage across zener diode is constant



$$i_{(R_2)} = \frac{V}{R} = \frac{50}{10\times10^3} = 5\times10^{-3}\,A$$

$$i_{(R_1)} = \frac{V}{R} = \frac{120-50}{5\times10^3} = \frac{70}{5\times10^3} 14\times10^{-3}\,A$$

$$\therefore i_{zenerdiode} = 14\times10^{-3} - 5\times10^{-3} = 9\times10^{-3}\,A = 9\,mA$$

17. **(c)** As we know, current density,

$$j = \sigma E = nev_d$$

$$\sigma = ne\frac{v_d}{E} = ne\mu$$

$$\frac{1}{\sigma} = \rho = \frac{1}{n_e e \mu_e} = \text{Resistivity}$$

$$= \frac{1}{10^{19}\times1.6\times10^{19} - 19\times1.6}$$

or $P = 0.4\,\Omega m$

18. **(d)** Initially Ge and Si are both forward biased so current will effectivily pass through Ge diode $\therefore V_\circ = 12 - 0.3 = 11.7$ V

And if "Ge" is revesed then current will flow through "Si" diode

$\therefore V_\circ = 12 - 0.7 = 11.3$ V

Clearly, $V_\circ$ changes by 11.7 – 11.3 = 0.4 V

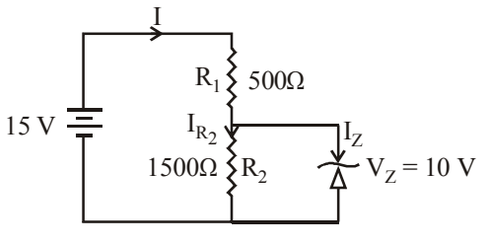
19. **(c)** Clearly from fig. given in question, Silicon diode is in forward bias.

$\therefore$ Potential barrier across diode

$\Delta V = 0.7$ volts

$$\text{Current, } I = \frac{V - \Delta V}{R} = \frac{3-0.7}{200} = \frac{2.3}{200} = 11.5mA$$

20. **(b)**



The voltage drop across R_2 is $V_{R_2} = V_Z = 10\,V$

The current through R_2 is

$$I_{R_2} = \frac{V_{R_2}}{R_2} = \frac{10\,V}{1500\Omega} = 0.667 \times 10^{-2}\,A$$

$$= 6.67 \times 10^{-3}\,A = 6.67\,mA$$

The voltage drop across R_1 is

$$V_{R_1} = 15V - V_{R_2} = 15V - 10V = 5V$$

The current through R_1 is

$$I_{R_1} = \frac{V_{R_1}}{R_1} = \frac{5\,V}{500\Omega} = 10^{-2}\,A = 10 \times 10^{-3}\,A = 10\,mA$$

The current through the zener diode is

$$I_Z = I_{R_1} - I_{R_2} = (10 - 6.67)mA = 3.3\,mA$$

21. **(a)** The conductivity of semiconductor

$$\sigma = e\,(\eta_e\mu_e + \eta_h\mu_h)$$

$$= 1.6 \times 10^{-19}(5 \times 10^{18} \times 2 + 5 \times 10^{19} \times 0.01)$$

$$= 1.6 \times 1.05 = 1.68$$

22. **(b)** Forward bias resistance $= \frac{\Delta V}{\Delta I} = \frac{0.1}{10 \times 10^{-3}} = 10\,\Omega$

Reverse bias resistance $= \frac{10}{10^{-6}} = 10^7\,\Omega$

Ratio of resistances $= \frac{\text{Forward bias resistance}}{\text{Reverse bias resistance}} = 10^{-6}$

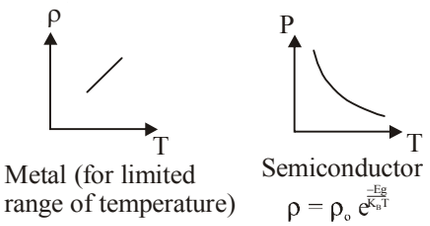
23. **(c)** Graph (p) is for a simple diode.

Graph (q) is showing the V Break down used for zener diode.

Graph (r) is for solar cell which shows cut-off voltage and open circuit current.

Graph (s) shows the variation of resistance h and hence current with intensity of light.

24. **(a)**



Metal (for limited range of temperature)

Semiconductor $\rho = \rho_o\, e^{\frac{-E_g}{K_B T}}$

25. **(c)** The minimum voltage range of DC source is given by

$V^2 = PR \quad \because P = 1$ watt, $R = 100\Omega$

$= 1 \times 100$

$\therefore V = 10$ volt.

26. **(d)** Using $U_{av} = \frac{1}{2}\varepsilon_0 E_0^{\,2}$

But $U_{av} = \frac{P}{4\pi r^2 \times c}$

$$\therefore \quad \frac{P}{4\pi r^2} = \frac{1}{2}\varepsilon_0 E_0^{\,2} \times c$$

$$E_0^2 = \frac{2P}{4\pi r^2 \varepsilon_0 c} = \frac{2 \times 0.1 \times 9 \times 10^9}{1 \times 3 \times 10^8}$$

$\therefore \quad E_0 = \sqrt{6} = 2.45 V/m$

27. **(a)** When positive terminal connected to A then diode D_1 is forward biased, current, $I = \frac{2}{5} = 0.4A$

When positive terminal connected to B then diode D_2 is forward biased, current, $I = \frac{2}{10} = 0.2A$

$$E_0^2 = \frac{2P}{4\pi r^2 \varepsilon_0 c} = \frac{2 \times 0.1 \times 9 \times 10^9}{1 \times 3 \times 10^8}$$

$\therefore \quad E_0 = \sqrt{6} = 2.45 V/m$

28. (d) Electrons in an unbiased *p-n* junction, diffuse from *n* -region i.e. higher electron concentration to *p*-region i.e. low electron concentration region.

29. **(a)**

For forward bias, p-side must be at higher potential than *n*-side. $\Delta V = (+)Ve$

30. **(d)** Energy band gap range is given by,

$$E_g = \frac{hc}{\lambda}$$

For visible region $\lambda = \left(4 \times 10^{-7} \sim 7 \times 10^{-7}\right)m$

$$E_g = \frac{6.6 \times 10^{-34} \times 3 \times 10^8}{7 \times 10^{-7}}$$

$$= \frac{19.8 \times 10^{-26}}{7 \times 10^{-7}}$$

$$= \frac{2.8 \times 10^{-19}}{1.6 \times 10^{-19}}$$

$E_g = 1.75\,eV$

31. **(d)** Here, $R = 4\,k\Omega = 4 \times 10^3\,\Omega$

$V_i = 60\,V$

Zener voltage $V_z = 10\,V$

$R_L = 2\,k\Omega = 2 \times 10^3\,\Omega$

Load current, $I_L = \frac{V_Z}{R_L} = \frac{10}{2 \times 10^3} = 5\,mA$

Current through R, $I = \frac{V_i - V_Z}{R}$

$= \frac{60-10}{4 \times 10^3} = \frac{50}{4 \times 10^3} = 12.5\,mA$

Fom circuit diagram,

$I = I_Z + I_L$

$\Rightarrow \quad 12.5 = I_Z + 5$

$\Rightarrow \quad I_Z = 12.5 - 5 = 7.5\,mA$

32. **(a)** For same value of current higher value of voltage is required for higher frequency hence (a) is correct answer.

33. **(a)** Here, diodes D_1 and D_2 are forward biased and D_3 is reverse biased.

Therefore current through R_3

$i = \frac{V}{R'} = \frac{6}{120} = \frac{1}{20}A = 50\,mA$

34. **(d)** Temperature coefficient of resistance is negative for pure semiconductor. And no. of charge carriers in conduction band increases with increase in temperature.

35. **(b)** The given circuit will work as half wave rectifier as it conducts during the positive half cycle of input AC.

Forward biased in one half cycle and reverse biased in the other half cycle].

36. **(a)** The current will flow through R_L when the diode is forward biased.

37. **(a)** Si and Ge are semiconductors but C is an insulator. In Si and Ge at room temperature, the energy band gap is low due to which electrons in the covalent bonds gains kinetic energy and break the bond and move to conduction band. As a result, hole is created in valence band. So, the number of free electrons is significant in Si and Ge.

38. **(c)** A crystal structure is made up of a unit cell arranged in a particular way; which is periodically repeated in three dimensions on a lattice. The spacing between unit cells in various directions is called its lattice constants. As lattice constants increases the band-gap (E_g), also increases which means more energy would be required by electrons to reach the conduction band from the valence band. Automatically E_c and E_v decreases.

39. **(b)** Van der Waal's bonding is attributed to the attractive forces between molecules of a liquid. The conductivity of semiconductors (covalent bonding) and insulators (ionic bonding) increases with increase in temperature.

Solid which is formed by covalent bond is not transparent to visible light and its conductivity increase with temperature.

40. **(c)** Relation between drift velocity and current is

$I = nAeV_d$

$\frac{I_e}{I_h} = \frac{n_e e A v_e}{n_h e A v_h}$

$\Rightarrow \frac{7}{4} = \frac{7}{5} \times \frac{v_e}{v_h}$

$\Rightarrow \frac{v_e}{v_h} = \frac{5}{4}$

41. **(b)** D_2 is forward biased.

D_1 is reversed biased. So, it will act like an open circuit.

So effective resistance of the circuit

$R = 4 + 2 = 6\Omega \qquad \therefore i = \frac{E}{R} = \frac{12}{6} = 2\ A$

42. **(d)** p-side connected to low potential and n-side is connected to high potential.

43. **(d)** Band gap = energy of photon of wavelength 2480 nm. So,

Band gap, $E_g = \frac{hc}{\lambda}$

$= \left(\frac{6.63 \times 10^{-34} \times 3 \times 10^8}{2480 \times 10^{-9}} \right) \times \frac{1}{1.6 \times 10^{-19}} eV$

$= 0.5\,eV$

44. **(a)** In forward biasing, the p type is connected to positive terminal and n type is connected with negative terminal. So holes from p region and electron from n region are pushed towards the Junction which reduces the width of depletion layer. Also, distance between diffused holes and electrons decrease, which decrease electric field hence barrier potential.

45. **(c)** Copper is a conductor and in conductor resistance decreases with decrease in temperature. Germanium is a semicon ductor. In semi-conductor resistance increases with decrease in temperature.

46. **(b)** When the temperature increases, certain bounded electrons become free which tend to promote conductivity. Simultaneously number of collisions between electrons and positive kernels increases which decrease the relaxation time.

47. **(a)** In reverse biasing the width of depletion region increases, and current flowing through diode is zero. Thus, electric field is zero at middle of depletion region.

48. **(c)** Pure silicon, at OK, will contain all the electrons in bounded state. The conduction band will be empty. So there will be no free electrons (in conduction band) and holes (in valence band).Therefore no electrons from valence band are able to shift to conduction band due to thermal agitation. Pure silicon will act as insulator.

49. **(c)** Specific resistance (resistivity) is given by

$$\rho = \frac{m}{ne^2\tau}$$

where n = no. of free electrons per unit volume

and τ = average relaxation time

For a conductor with rise in temperature n increases. Increase in temperature results increase in number of collision between free electrons due to which relaxation time T decreases. But the decrease in τ is more dominant than increase in n resulting an increase in the value of ρ .

For a semiconductor with rise in temperature, n increases and τ decreases. But the increase in n is more dominant than decrease in τ resulting in a decrease in the value of ρ.

ALTERNATE SOLUTION

$\rho_2 = \rho_1(1+\alpha\Delta T)$

For conductor α is positive

$\therefore \rho_2 > \rho_1$ for ΔT positive i.e., increase in temperature.

For semi conductor α is negative

$\therefore \rho_2 < \rho_1$ for ΔT positive.

50. **(c)** In insulators, valence band is completely filled while conduction band is empty. The energy band gap is maximum in insulators.

51. **(150)**

At $V_{CE} = 10$ V and $I_C = 4$ mA

Change in base current, $\Delta I_B = (30-20) = 10\ \mu A$

Change in collector current, $\Delta I_C = (4.5-3) = 1.5$ mA

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right) = \frac{1.5\ mA}{10\mu A} = 150$$

52. **(Bonus)** $\beta = \frac{\Delta i_c}{\Delta i_b} = \frac{200-100}{10-5} = 20$

$$\text{Voltage gain} = \beta\frac{R_2}{R_1} = \frac{20\times100\times10^3}{100} = 20\times10^3$$

$$\text{Power gain} = \beta^2\frac{R_2}{R_1} = 20^2\left(\frac{100\times10^3}{100}\right) = 4\times10^5$$

53. **(a)** Power gain $= 60 = 10\log\left(\frac{P_0}{p_i}\right)$

$$\Rightarrow 6 = \log\left(\frac{P_0}{p_i}\right)$$

$$\Rightarrow \frac{P_0}{p_i} = 10^6$$

$$= \beta^2\left(\frac{R_{out}}{R_{in}}\right)$$

$$\Rightarrow 10^6 = \beta^2\left(\frac{10000}{100}\right) \quad [\text{as } R_{out} = 10,000\Omega\ R_{in} = 100\Omega]$$

$$\Rightarrow \beta = 100$$

54. **(b)** $\beta = \frac{\Delta lc}{\Delta lb} = \frac{3\times10^{-3}}{15\times10^{-6}} = 200$

We have $\frac{V_0}{V_i} = \beta\frac{R^2}{R_1}$

or $\frac{V_0}{V_i} = 200\left(\frac{1000}{R_1}\right)$

If $R_1 = 0.67\text{k}\Omega \Rightarrow \frac{V_0}{V_i} = 300$

55. **(a)** Given, $\beta = 250$

Voltage gain, $\frac{V_{CC}}{V_B} = \beta\frac{R_C}{R_B}$

$$\frac{10}{V_B} = 250\times\frac{10^3}{R_B}$$

$$\therefore \frac{V_B}{R_B} = \frac{1}{25\times10^3} = 40\mu A$$

56. **(a)** At saturation, $V_{CE} = 0$

$$V_{CE} = V_{CC} - I_C R_C$$

$$\Rightarrow \quad I_C = \frac{V_{CC}}{R_c} = 5\times10^{-3}\text{ A}$$

Current gain,

$$\beta_{dc} = \frac{I_C}{I_B}$$

$$I_B = \frac{5\times10^{-3}}{200} = 25\ \mu A$$

At input side

$$V_{BB} = I_B R_B + V_{BE}$$
$$= (25\text{ mA})(100\text{ k}\Omega) + 1\text{V}$$
$$V_{BB} = 3.5\text{ V}$$

57. **(d)** Curent gain $\beta = \frac{\Delta I_C}{I_B}$

Voltage gain A_v = Current gain × Resistance gain $= \beta\frac{R_L}{R_{BE}}$

Power gain A_p = (Current gain)^2 × Resistance gain

$$= \beta^2\frac{R_L}{R_{BE}}$$

58. **(b)** Given, current gain of CE amplifier $\beta = 69$, $I_E = 7$ mA

or $\frac{I_C}{I_B} = 69$

We know that, $\alpha = \frac{\beta}{1+\beta} = \frac{69}{70} = \frac{I_C}{I_E}$

$I_C = I_E \times \frac{69}{70} = \frac{69}{70} \times 7$

Collector current, $I_C = 6.9$ mA

59. **(b)** In common emitter configuration for *n-p-n* transistor input and output signals are 180° out of phase *i.e.,* phase difference between output and input voltage is 180°.

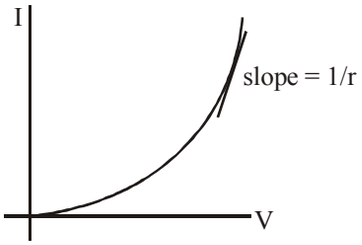
60. **(b,d)** We know that $\alpha = \frac{I_c}{I_e}$ and $\beta = \frac{I_c}{I_b}$

Also $I_e = I_b + I_c$

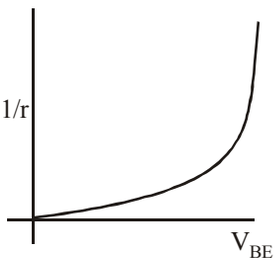
$\therefore \alpha = \frac{Ic}{I_b + I_c} = \frac{\frac{I_c}{I_b}}{1+\frac{I_c}{I_b}} = \frac{\beta}{1+\beta}$

Option (b) and (d) are therefore incorrect.

61. **(c)**



$\Rightarrow$

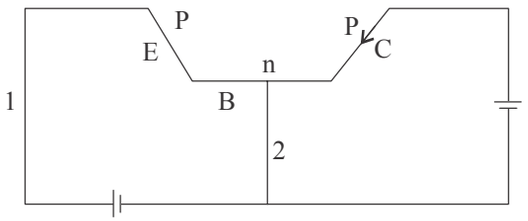


62. **(c)** For C.B. configuration $\frac{r_i}{r_o} \cong 0.1\Omega$

For CE and CC-configuration

$\frac{r_i}{r_0} \approx 1\Omega$.

63. **(c)** Connecting circuit according to question, it is clear



+ve terminal 1, –ve terminal 2, resistance high.

64. **(c)** In the given question, A, B and C refer base, collector and emitter respectively.

65. **(b)** It is a *p-n-p* transistor with *R* as base.

66. **(a)** Collector current, $I_C = 5.488$ mA,

Emitter current $I_e = 5.6$ mA

$\alpha = \frac{I_c}{I_e} = \frac{5.488}{5.6}$,

$\beta = \frac{\alpha}{1-\alpha} = 49$

67. **(d)** In common base amplifier circuit, input and output voltage are in the same phase. So, the phase difference between input voltage signal and output voltage signal is zero.

68. **(c)** In npn transistor, electrons moves from emitter to base.

69. **(d)** In common emitter configuration for transistor amplifier current gain

$A_i = \frac{-h_{fe}}{1+b_{oe}R_L}$

Where h_{fe} and h_{oe} are hybrid parameters.

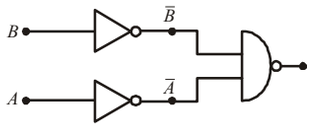
$\therefore A_i = \frac{-50}{1+25\times10^{-6}\times1\times10^{3}}$

$= -48.78$

70. **(a)** Emitter main function is to supply the majority charge carrriers towards the collector. Therefore emitter is most heavily doped.

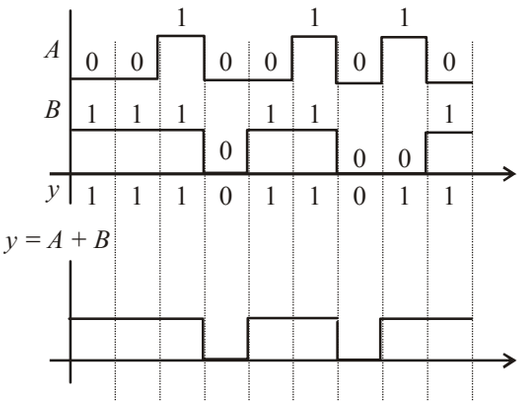
71. **(a)** Boolean expression,

$y = \overline{\bar{A}\cdot\bar{B}} = \bar{\bar{A}} + \bar{\bar{B}} = A + B$



Truth table :

A	B	Y
0	1	1
1	0	1
0	0	0
1	1	1



72. **(c)** When two inputs of NAND gate is shorted, it behaves like a NOT gate so boolen equation will be

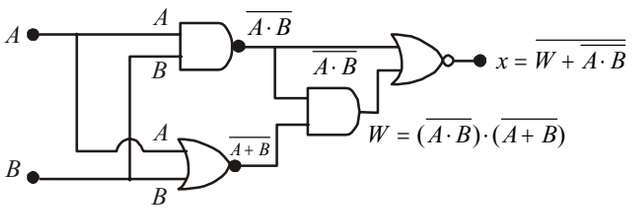
$y = \overline{\overline{A} + \overline{B} + \overline{C}}$

$y = A \cdot B \cdot C$

A	B	C	
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	1

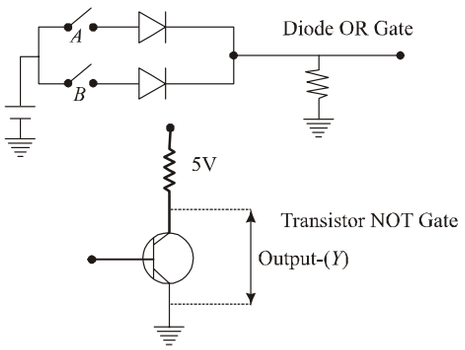
Thus, whole arrangement behaves like a AND gate.

73. **(a)**



A	B	$\overline{A \cdot B}$	$\overline{A+B}$	$W = (\overline{A \cdot B}) \cdot (\overline{A+B})$	$Q = W + \overline{A \cdot B}$	$\overline{Q} = x$
1	0	1	0	0	1	0
0	1	1	0	0	1	0
1	1	0	0	0	0	1
0	0	1	1	1	0	0

74. **(d)**

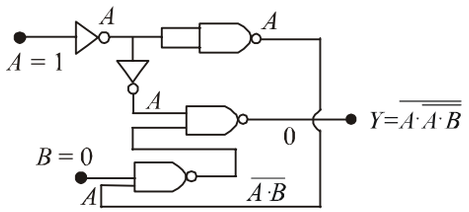


OR + NOT → NOR Gate

Hence Boolean relation at the output stage – Y for the circuit,

$Y = \overline{A+B} = \overline{A}.\overline{B}$

75. **(a)**



$Y = \overline{\overline{AB}.A} = \overline{\overline{AB}} + \overline{A} = AB + \overline{A}$

For $A = 1, B = 0$

$Y = (1) \times 0 + 0$

$\Rightarrow Y = 0 + 0 = 0$

76. **(d)** A logic gate is reversible if we can recover input data from the output. Hence NOT gate.

77. **(c)**

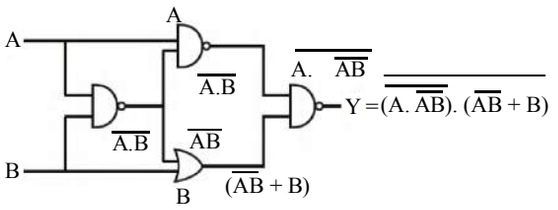
A	B	(A + B)	(A + B). A	$\overline{(A+B).A}$
0	0	0	0	1
0	1	1	0	1
1	0	1	1	0
1	1	1	1	0

78. **(b)** Truth table →

The output is of OR-gate

A	B	$\overline{A}$	$\overline{B}$	$\overline{\overline{A}.\overline{B}}$
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

79. **(c)**



$$Y=\left(\overline{A\cdot\overline{AB}}\right)+\left(\overline{\overline{AB}+B}\right)$$

$$=A\cdot\overline{AB}+AB\cdot\overline{B}$$

$$=A\cdot\left(\overline{A}+\overline{B}\right)+AB\cdot\overline{B}$$

$$=A\overline{B}$$

80. **(c)** From the given logic circuit,

$p=\overline{x}+y$

$Q=\overline{\overline{y}.x}=y+\overline{x}$

Output, $R=\overline{P+Q}$

To make output 1

P + Q must be '0'

So, x = 1, y = 0

81. **(c)** Truth table of the circuit is as follows

x	y	$\overline{x}$	$a=x.y$	$b=\overline{x}.y$	$z=\overline{a.b}$
0	0	1	0	0	1
0	1	1	0	1	1
1	0	0	0	0	1
1	1	0	1	0	1

82. **(a)** In case of an 'OR' gate the input is zero when all inputs are zero. If any one input is ' 1', then the output is '1'.

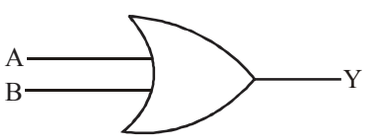
83. **(c)** Truth table for given logical circuit

a	b	(a + b)	c	Y = (a + b) .c
0	0	0	0	0
0	1	1	1	1
1	0	1	1	1
1	1	1	0	0

Output of OR gate must be 1 and c = 1

So, a = 1, b = 0 or a = 0, b = 1.

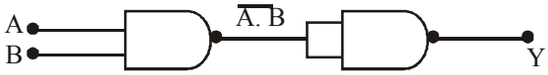
84. **(a)** It represents OR-Gate.



A	B	A + B = Y
0	0	0
0	1	1
1	0	1
1	1	1

85. **(a)** AND Gate

86. **(a)**



$$Y=\overline{\overline{AB}.\overline{AB}}=\overline{\overline{AB}}+\overline{\overline{AB}}=AB+AB=AB$$

In this case output Y is equivalent to AND gate.

87. **(a)** For circuit 1

$$A\,.\,B=\overline{Y+\overline{A}}=C$$

A	B		$\overline{Y+\overline{A}}$	= C
0	0	0	1	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

88. **(a)** In the given system all four gate is NOR gate

Truth Table

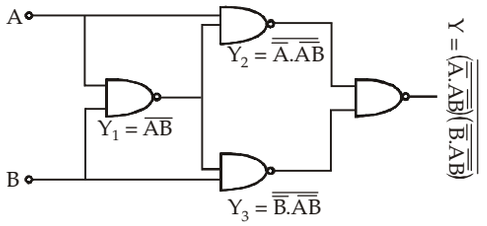
A	B	$(y'=\overline{A+B})$	$y''=(\overline{A+y'})$	$y'''=(A+y'')$	$y=\overline{y''+y'''}$
0	0	1	0	0	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

i.e.,

A	B	y
0	0	1
0	1	0
1	0	0
1	1	1

89. **(a)** The output at C corresponds to A NAND B or $\overline{A\cdot B}=C$

90. **(a)**



By expanding this Boolen expression

$Y=A.\overline{B}+B.\overline{A}$

Thus the truth table for this expression should be (a).

91. **(c)** Truth table is as shown :

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$	$\overline{\overline{A}+\overline{B}}$
0	0	1	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1

Thus the combination of two NOT gates and one NOR gate is equivalent to a AND gate.

92. **(a)** NOR gate is the combination of NOT and OR gate.

Boolean expression for NOR gate is

$Y = \overline{A + B}$

93. **(b)** When either of A or B is 1 i.e. closed then lamp will glow.

In this case, Truth table

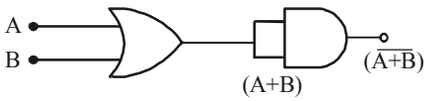
Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

This represents OR gate.

94. **(b)** When both inputs of NAND gate are jointed to form a single input, it behaves as NOT gate

OR + NOT = NOR.

$\left(\overline{A + B}\right)$ = NOR gate



95. **(a)** The final boolean expression of these gates is,

$X = \left(\overline{\bar{A}.\bar{B}}\right) = \bar{\bar{A}} + \bar{\bar{B}} = A + B \Rightarrow$ OR gate

It means OR gate is formed.

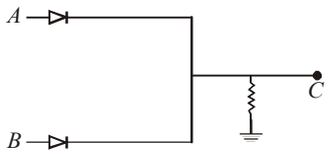
96. **(d)** The final boolean expression

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$Y = (\overline{\bar{A} + \bar{B}}) = \bar{\bar{A}}.\bar{\bar{B}} = A \cdot B$.

Thus, it is an AND gate for which truth table is

97. **(d)**



The truth table for the above circuit is :

A	B	C
1	1	1
1	0	1
0	1	1
0	0	0

when either A or B conducts, the gate conducts. It means $C = A + B$ which is for OR gate.